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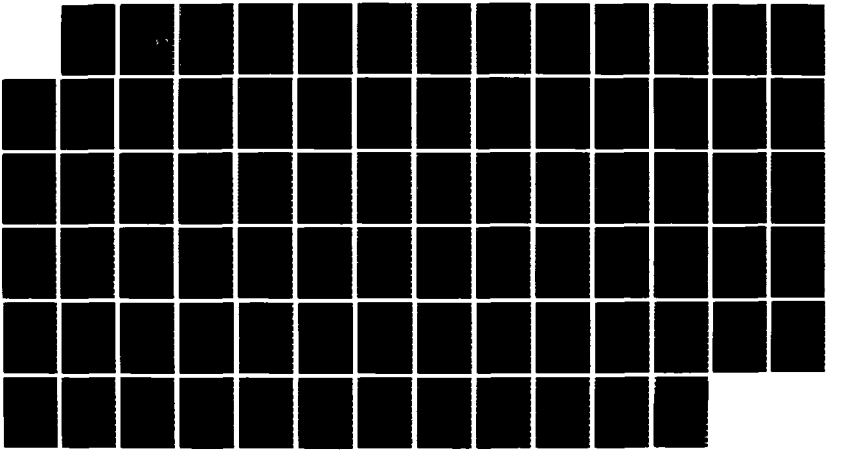

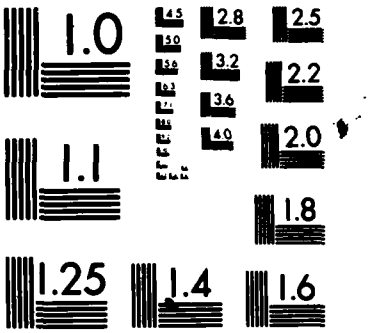

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DELAY MODELING OF BIPOLAR ECL/EFL CIRCUITS

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Andrew Tien Yang

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DELAY MODELING OF BIPOLAR ECL/EFL CIRCUITS

BY

ANDREW TIEN YANG

B.S., University of California, Berkeley, 1983

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering
in the Graduate College of the
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ABSTRACT

This thesis deals with the development of a delay-time model for timing simulation of large circuits consisting of Bipolar ECL (Emitter-Coupled Logic) and EFL (Emitter-Follower-Logic) networks. This model can provide adequate information on the performance of the circuits with a minimum expenditure of computation time. This goal is achieved by the use of proper circuit transient models on which analytical delay expressions can be derived with accurate results. The delay-model developed in this thesis is general enough to handle complex digital circuits with multiple inputs or/and multiple levels. The important effects of input slew rate are also included in the model.

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TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

With the advances in VLSI technology, CAD tools have become virtually indispensable at various steps in the design process. One of the key CAD tools is the circuit simulator which simulates the electrical behavior of the circuit for the purpose of verifying the performance of the design. Two criteria, namely, the *simulation cost* (measured by the CPU time and memory space allocated) and the *accuracy*, govern the effectiveness of a circuit simulator. Conventional circuit simulators, such as SPICE [8], were designed for the cost-effective analysis of circuits containing a few hundred transistors or less. They have high accuracy, but the simulation cost is high. As the size of the circuit increases, using these simulators is no longer practical. There exists another type of circuit simulators, called the **digital simulators**, which view the whole circuit as a digital network consisting of structured subnetworks (gates, function blocks, etc) with signals occupying discrete states. They are known for their fast simulation time and capability to handle large circuits. However, most of them provide very poor delay information, or sometimes, none at all. Therefore, a need exists for simulators that provide adequate circuit analysis at reasonable simulation cost. A cost-effective approach is to incorporate better delay models into digital simulators, so that **logic** and **timing** simulations can be done simultaneously at reasonable cost.

An approach to deriving delay models for fast timing analysis has been used in MOSTIM [1] and OVSIIM [7] for timing simulation of MOS VLSI circuits. MOSTIM, a switch-level simulator, incorporates delay operators which are characterized by delay functions computed for a set of standard circuit **primitives** and stored in tables. This *preprocessing* step involves the use of an accurate circuit simulator, such as SPICE, to simulate each primitive. OVSIM, on the other hand, expresses the delay as a function of device and circuit parameters, and does not require the use of a

circuit simulator as a preprocessing step.

Despite the increasing market share of MOS IC's, *bipolar digital circuits* still remain very attractive in the industry. For *high performance* applications, bipolar IC's remained to be the technology unchallenged. As a result, a need exists for verifying the logic and timing behaviors of the design directly from circuit level descriptions without having to carry out detailed circuit simulations. Recently, some results on design aids for bipolar ECL (Emitter-Coupled Logic) and EFL (Emitter-Follower Logic) circuits. have been reported. In reference [2], an approach is described which converts ECL/EFL circuits to logic gate descriptions. A *function block* can be formed by the interconnections of these logic gates. To obtain delay information, detailed circuit simulations are performed on each function block. Then, a means for calculating circuit delays for an entire chip is carried out by including the effects of metal interconnections between functional blocks and to the I/O buffers. The approach has three shortcomings. First, the recognition process requires proper sequencing of the recognition steps. Second, the logic block descriptions do not have one-to-one correspondence with the actual circuit. Third, a large number of circuit simulations of the different function blocks by conventional circuit simulators are essential for delay calculations. Obviously, a heavy burden is placed on the circuit designer to acquire adequate timing informations.

In reference [3], another approach to logic simulation of bipolar digital circuits is based on the development of a switch-level model of the transistor and on the representation of the circuit by a switch-graph. This method can extract a gate-level functional description of the circuit from a circuit level description created by a layout analysis program. Logic simulation can then be performed using either extracted logic expressions or the switch-graph model. Timing analysis, on the other hand, is not performed since no delay information is included. However, the approach forms a good basis for fast timing analysis if one can incorporate an accurate delay model.

It is, therefore, the intention of this thesis to provide an accurate delay model for the timing simulation of bipolar digital circuits, specifically, ECL and EFL logic families. This delay model can

then be incorporated into the switch-level logic simulation program as delay operators to perform the timing analysis. The delay model should have the following attributes.

1. SPICE simulation is not required at any time.

2. High accuracy compared with SPICE (within 15%) is required.

3. Numerical iterations should be avoided to save cost.

This thesis is organized as follows. In Chapter 2, background material for bipolar transistors is reviewed. Emphasis is particularly placed on the charge-control model for transient analysis. Then, a basic ECL gate is presented along with its *delay-sensitive* parameters. In Chapter 3, a very important aspect of delay computation, namely, the intrinsic delay (τ_{in}), is covered. The effects of input slew rate on the delay computation are also discussed. In Chapter 4, the topics of I-V conversion delay and emitter-follower delay are covered. These delays are lumped as the extrinsic delay (τ_{ext}). Interconnection delay, or the loading effect, is also included in this chapter. In Chapter 5, our results for the basic gate are extended to more complicated multiinputs, multilevel ECL circuits. In Chapter 6, the delay model is implemented and evaluated for several bipolar circuits. Conclusions along with some suggestions for future research are presented in Chapter 7.

CHAPTER 2

BACKGROUND

2.1. Introduction

In this thesis, we will be mainly concerned with NPN bipolar transistors operated under either *forward active* mode or *cut-off* mode. An NPN transistor is shown in Fig. 2.1 with the indicated voltage and current conventions. It is composed of a pair of back-to-back diodes. Under the forward active mode, the B-E junction is forward-biased ($V_{be} \geq V_{bcon}$), and the B-C junction is reverse-biased ($V_{bc} < V_{bcon}$). When the transistor is in the cutoff mode, both the B-E junction and the B-C junction are reversed-biased.

For transient analysis, charge-storage effects are of paramount importance. If there were no charge storage, then the device would take no time to switch. That is, current can be changed in

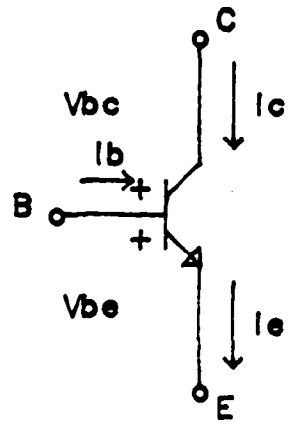

Figure 2.1 *npn* transistor

zero time. The two forms of charge storage for a bipolar transistor are the neutral region **excess minority-carrier storage** and the depletion region **majority-carrier space charge storage**. As shown later, successful modeling of these two charge storage effects enables us to derive the delay functions of ECL logic. Most of the background materials covered in this chapter can be found in many excellect books [4], [5] and [6].

2.2. Excess minority-carrier storage

When the transistor operates in the forward active mode, electrons in the emitter region are injected into the base region as the excess minority carriers. These carriers are then quickly swept into the collector region. The distribution of these excess minority carriers in the base region leads to diffusion current flow. A distribution of excess minority carriers of a forward active transistor is shown in Fig. 2.2.

This excess minority-carrier charge storage gives rise to the capacitorlike behavior and is usually called the **diffusion capacitor**, C_{dif} . Storage and extraction of charges from C_{dif} contribute a significant portion to the switching delay.

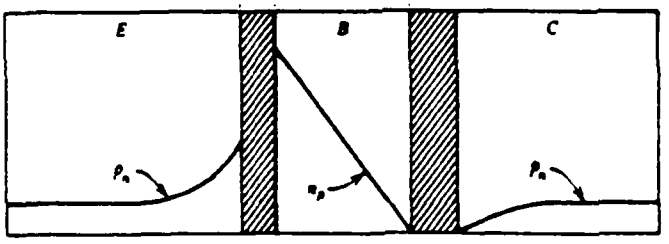

Figure 2.2 Minority carrier distribution in the base

For an uniformly doped base, the total charges contributed by excess minority carrier storage (Q_f) can be derived from the distribution profile in Fig. 2.2. From the law of junction [4], the minority carrier concentration at the edge of the depletion region of B-E junction is

$$n'b(0) = nb_o(e^{\frac{Vbe}{Vt}} - 1) \tag{2.1}$$

where nb_o is the minority carrier concentration in the base and V_t is the thermal voltage. The collector current is mainly the diffusion current, and is given by

$$Ic = qAD_b \frac{dn'b(x)}{dx} \tag{2.2}$$

or

$$Ic = qAD_b \frac{n'b(0)}{W} \tag{2.3}$$

Substituting Eq.(2.1) into Eq.(2.3), we obtain

$$Ic = qAD_b \frac{nb_0}{W}(e^{\frac{Vbe}{Vt}} - 1) \tag{2.4}$$

where A is the cross-sectional area, D_b is the diffusion constant in the base and W is the effective base width. From Fig. 2.2, the total excess minority carrier base charge is

$$Q_f = qAW\frac{n'b(0)}{2} \tag{2.5}$$

Substituting Eq.(2.1) into Eq.(2.5), we get

$$Q_f = qAW\frac{nb_0}{2}(e^{\frac{Vbe}{Vt}} - 1) \tag{2.6}$$

If Eq.(2.4) is combined with Eq.(2.6), we can describe Q_f in terms of Ic as

$$Q_f = \frac{W^2}{2D_b}Ic \tag{2.7}$$

or,

$$Q_f = \tau_f \, Ic \tag{2.8}$$

Equation (2.8) is a very important equation relating Ic and Q_f. τ_f is the *forward transit time* for the device and is a technology-dependent parameter. For the transient properties of bipolar transistor, Eq.(2.8) can be expressed as

$$i_c(t) = \frac{Q_f(t)}{\tau_f} \tag{2.9}$$

For the base current,

$$i_b(t) = \frac{Q_f(t)}{\tau_{bf}} + \frac{dQ_f}{dt} \tag{2.10}$$

and

$$\beta_f = \frac{\tau_{bf}}{\tau_f} \tag{2.11}$$

The first steady-state term in Eq.(2.10) includes the loss of minority carriers in the base region. The second transient term is introduced to account for the time rate of change of Q_f in the neutral base region. By combining Eq.(2.9) and Eq.(2.10) we have

$$i_e(t) = \frac{Q_f(t)}{\tau_f} + \frac{Q_f(t)}{\tau_{bf}} + \frac{dQ_f}{dt} \tag{2.12}$$

Equations (2.9), (2.10) and (2.12) [5] constitute a set of *charge-control* equations describing the steady-state and transient behaviors of a bipolar transistor in the *forward active* mode.

2.3. Majority-carrier space charge storage

A bipolar transistor is composed of two back-to-back pn junctions. A reversed bias across a pn junction exposes fixed donor and acceptor charges by extracting compensating free charges. This charge storage in the depletion region gives rise to the capacitorlike behavior and is usually denoted as **junction capacitor**, C_j, or **depletion capacitor**. Junction capacitors are the main cause of

switching delay for bipolar digital circuits. From basic device physics [5],

$$Q_j = A\left|2\epsilon_{si}\, q \frac{N_a N_d}{N_a + N_d}\right|^{1/2} (\phi_0 - V)^m \tag{2.13}$$

where ϵ_{si} is the permittivity of silicon and ϕ_0 is the built-in potential ($\approx$0.7V) for the pn junction. N_a and N_d are the doping concentrations of p-type and n-type materials, respectively. We may define the junction capacitance as

$$C_j = \frac{dQ_j}{dV} = A\left|\frac{\epsilon_{si}\, q}{2} \frac{N_a N_d}{N_a + N_d}\right|^{1/2} \frac{1}{(\phi_0 - V)^m} \tag{2.14}$$

or

$$C_j = \frac{C_{j0}}{\left|1 - (V/\phi_0)\right|^m} \tag{2.15}$$

where C_{j0} is the zero-biased junction capacitance, and m is the grading coefficient. For the abrupt junction derived above, m is 1/2. Usually, m is between 1/2 and 1/3. Note that the depletion capacitor is nonlinear and voltage dependent. An important simplification can be made by using the equivalent voltage-independent capacitance C_{eq}.

$$C_{eq} = K_{eq} C_{j0} \tag{2.16}$$

where

$$K_{eq} = \frac{-2\phi_0^{1/2}}{V_2 - V_1}\left|(\phi_0 - V_2)^{1/2} - (\phi_0 - V_1)^{1/2}\right| \tag{2.17}$$

2.4. Modeling for delay extraction

Modeling for transient analysis is an indispensable step for the derivation of delay functions, since all the transient effects can be completely understood with the aid of proper models. Based on the charge storage effects discussed above, a proper model for both dc and transient effects of the device is shown in Fig. 2.3, where

$$Q_{BE} = \tau_f \, Ic + C_{je0} \int_0^{V_{BE}} \left| 1 - \frac{V}{\phi_e} \right|^{-me} dV \tag{2.18}$$

$$Q_{BC} = \tau_r \, Ie + C_{jc0} \int_0^{V_{BC}} \left| 1 - \frac{V}{\phi_c} \right|^{-mc} dV \tag{2.19}$$

Note that in Fig. 2.3, r_c r_e and r_b are the parasitic resistances determined by the process and the size of the transistor.

Although we now have a full dc and transient model, it still appears to be quite cumbersome to apply. Note that for ECL logic, we are interested in the device operating only in either the forward active or cutoff modes. Therefore, further simplifications can be made based on the following two important observations.

First, from Eq.(2.9), we can conclude that, when the transistor is in the cutoff mode, Q_f is negligible, and Q_{jc} and Q_{je} are the dominant charges. Therefore, a dc and transient model can be simplified to the one shown in Fig. 2.4.

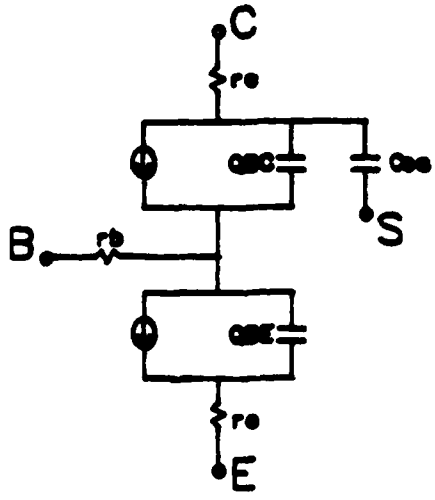

Figure 2.3 Complete dc and ac Model

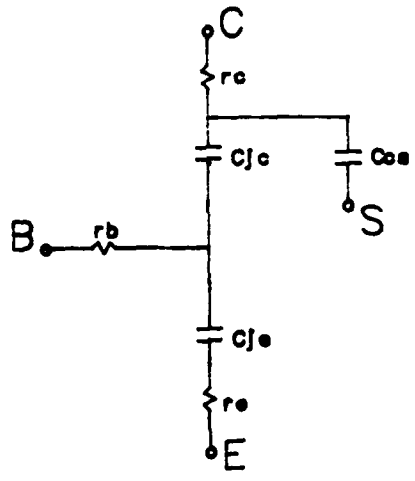

Figure 2.4 Model for device under cutoff mode

Second, from Eq.(2.13), we can conclude that, when the transistor is on, Q_{je} is negligible, and Q_f and Q_{jc} are the dominant charges. Therefore, a dc and transient model can be simplified as shown in Fig. 2.5. These two important observations can be easily illustrated by a plot of stored charges versus V (junction voltage) shown in Fig. 2.6.

2.5. Basics of ECL logic

For the remaining part of this chapter, an introduction to ECL logic will be given, including a *firstlook* at ECL delay.

2.5.1. Configuration and operation

ECL logic is presently the fastest commercially available form of digital IC, with typical propagation delay time of less than 0.5 ns and clock rates exceeding 2 GHZ. The reasons for the fast ECL logic are

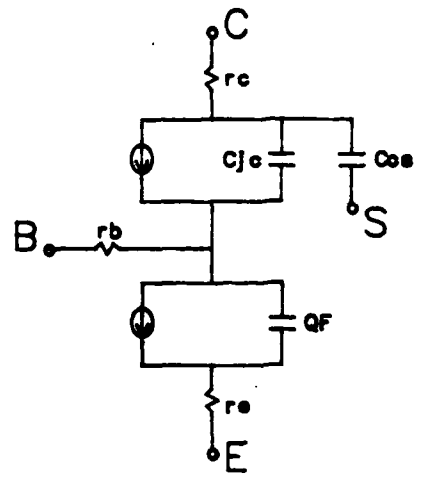

Figure 2.5 Model for device under forward bias mode

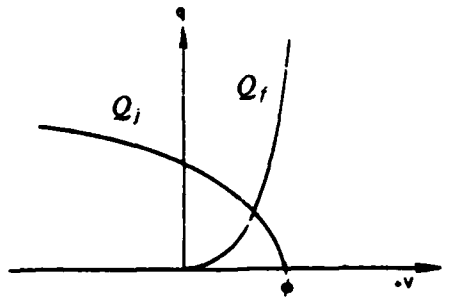

Figure 2.6 Plot of Q_j and Q_f versus applied voltage

(1) **Current switch operation** reduces the need for full-swing input to turn 'ON', or to turn 'OFF' an input transistor.

(2) **Nonsaturated logic** reduces base charge storage.

(3) **Small logic swing** enables fast charge-up and discharge.

(4) **High drive** capability provided by emitter followers at the outputs reduces the interconnection delays.

(5) **High power**, provided by the bipolar I-V characteristic, reduces the delay to charge up or discharge the parasitic capacitance. (low RC constant)

A basic two-input ECL gate is shown in Fig. 2.7. The steering current, I_{tree} , is provided by a simple transistor current source. The *steering actions* of I_{tree} are controlled by the differential inputs (one-sided, or symmetrical). Output nodes can be "pulled up", or, "pulled down," depending on whether I_{tree} is steered away, or steered to the output path. Output swing is related to the ratio of Rc and Rs, and is expressed as

$$V_{swing} = \phi = \frac{Rc}{Rs}(V_{cs} - V_{beon} - VEE) \tag{2.20}$$

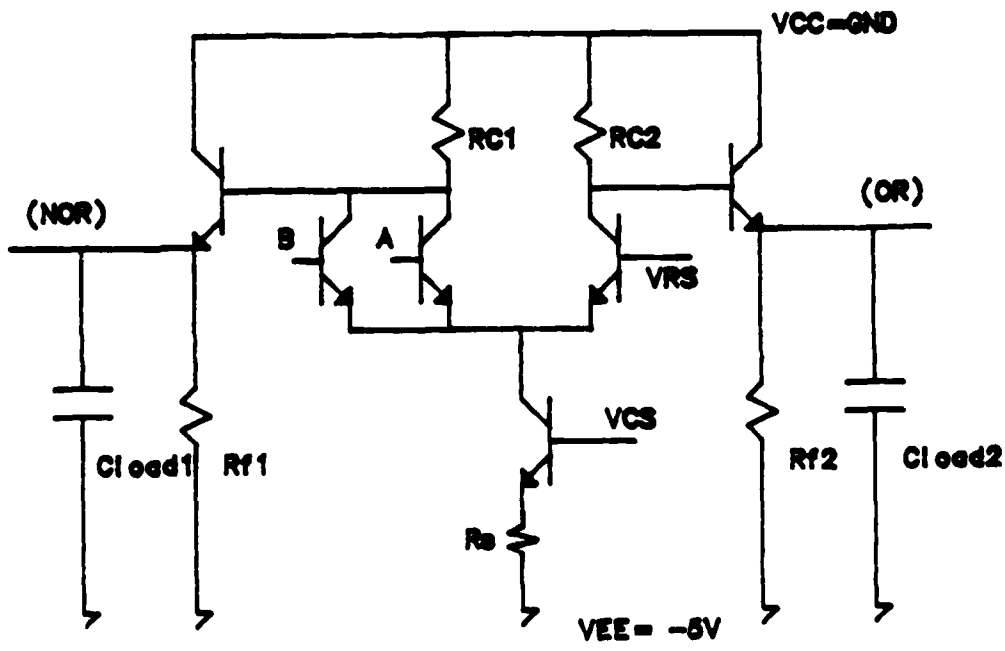

Figure 2.7 A two-input ECL gate

ϕ is an important quantity and is approximately equal to V_{beon} . V_{cs} and V_{rs} are referenced voltages generated by the *heart* of the circuit, the *ECL generator*. The logics realized by this basic two-input gate are (OR) and (NOR). Note that the outputs are complementary.

2.5.2. Firstlook at the delay

A basic single-input ECL with all the associated parameters is shown in Fig 2.8. It is simulated by SPICE and a typical output is shown in Fig. 2.9. The emitter follower resistor, R_f , has a value of 1800 ohms with a loading capacitance, C_{load} , of 1.0 pF. Its total power dissipation is 40 mW with steering current of 4.0 mA. The device parameters for the steering transistors are

β_f =75 C_{cs} =0.5 pF C_{jc} =0.2 pF rb=40 ohms Me=0.383 τr=2.50 ns

re=10 ohms C_{je} =0.25 pF τf=0.08 ns Is=2.0E-16A Mc=0.500 rc=15 ohms

By varying a single parameter, while keeping others fixed, one can examine the relative sensitivity of delay to that parameter. A good preliminary investigation of switching delays (as

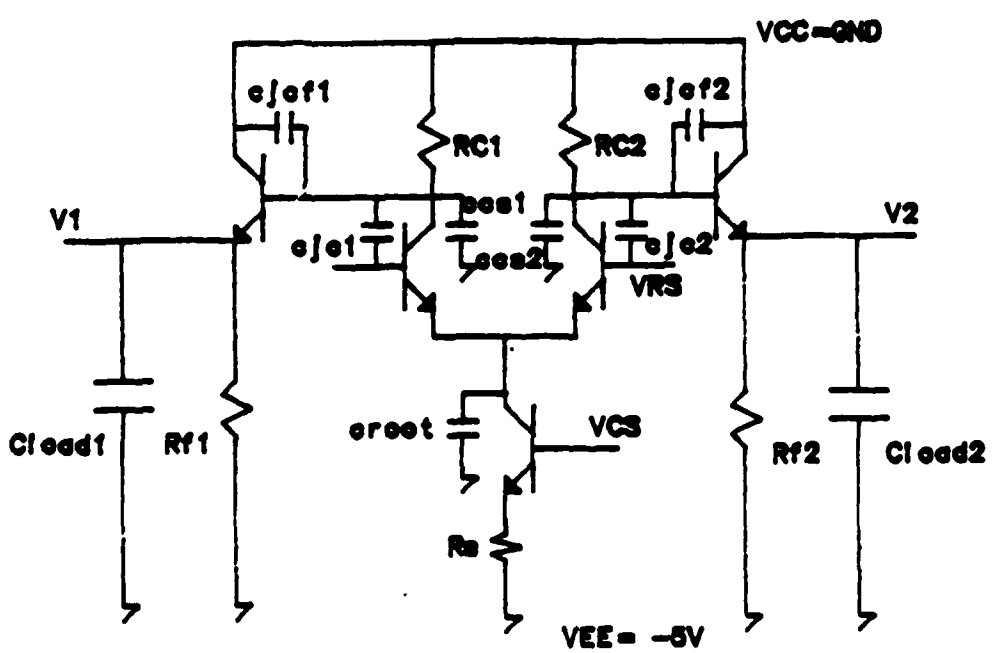

Figure 2.8 A basic ECL gate with the associated parasitics

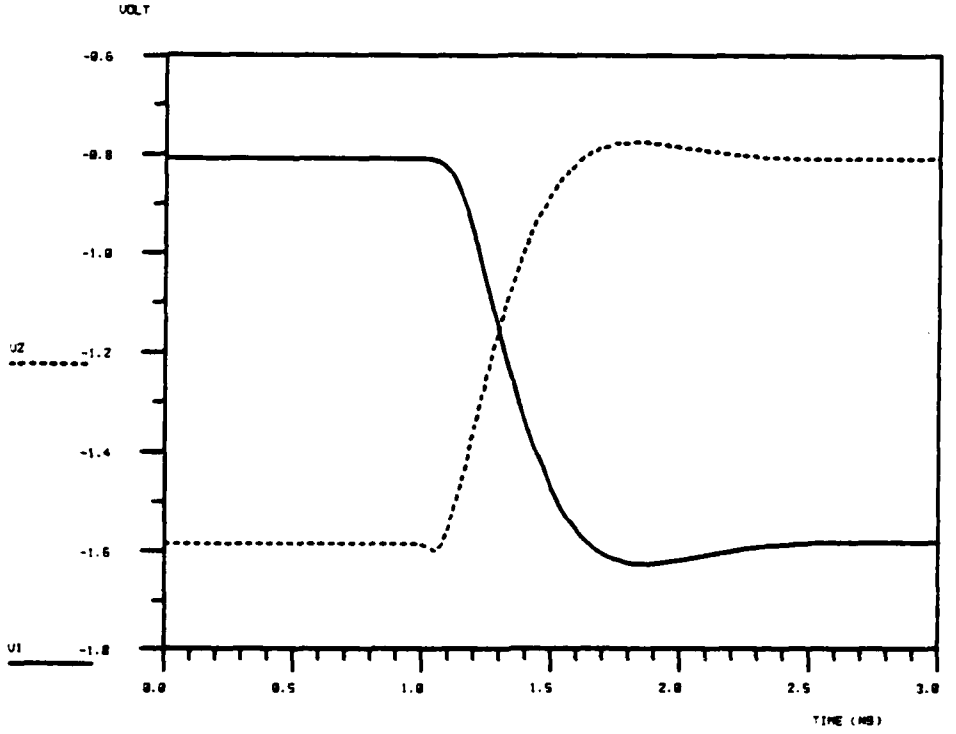

Figure 2.9 Typical switching outputs

functions of various parameters) can thus be obtained. To have a feeling of the degree of dependence of delay on each parameter for just a simple ECL gate, several graphs are included here.

From Fig. 2.10 to Fig 2.19, delays are plotted from page 17 to page 21, respectively, for

τ_f : 0.01 ns, 0.05 ns, 0.10 ns, 0.30 ns, 0.60 ns. (Fig. 2.10)

rb: 10 ohms, 40 ohms, 80 ohms, 160 ohms, 320 ohms. (Fig. 2.11)

Rc: 100 ohms, 200 ohms, 400 ohms, 800 ohms, 1600 ohms. (Fig. 2.12)

T_{slew} : 0.0 ns, 0.5 ns, 1.0 ns, 2.0 ns. (Fig 2.13)

C_{jc} : 0.1 pF, 0.2 pF, 0.4 pF, 0.8 pF, 1.6 pF. (Fig 2.14)

C_{cs} : 0.1 pF, 0.2 pF, 0.4 pF, 0.8 pF, 1.6 pF. (Fig 2.15)

C_{iso} : 0.1 pF, 0.2 pF, 0.4 pF, 0.8 pF, 1.6 pF. (Fig 2.16)

C_{jcf} : 0.1 pF, 0.2 pF, 0.4 pF, 0.8 pF, 1.6 pF. (Fig 2.17)

R_f : 500 ohms, 1000 ohms, 2000 ohms, 4000 ohms, 8000 ohms. (Fig 2.18)

C_{load} : 0.5 pF, 1.0 pF, 2.0 pF, 4.0 pF, 8.0 pF. (Fig 2.19)

Delays for the plots above are extracted by using the SPICE program. Several notations used above need to be clarified. C_{jcf} and R_f are the base-collector junction capacitor and pull-down resistor for the emitter follower, respectively. C_{root} is the capacitance associated with the current source at the *root* of the differential pair. C_{load} is the loading capacitance at the output of the emitter follower and its value depends on the interconnection capacitance and the number of *fanouts*. T_{slew} is the input slew rate. Based on the results obtained above, one can conclude that the ECL switching delay, τ_d, has *first-order* dependences on many parameters and can be expressed as

$$\tau_d \approx \mathbf{F}(\tau_f, \mathbf{rb}, \mathbf{Rc}, \mathbf{C_{jc}}, \mathbf{C_{cs}}, \mathbf{C_{root}}, \mathbf{T_{slew}}, \mathbf{C_{jc}}\,\mathbf{f}, \mathbf{Rf}, \mathbf{C_{load}})_{\text{first-order}} \qquad (2.21)$$

In addition to the first-order dependences specified by Eq.(2.19), τ_d also has *second-order* dependences on β_f, C_{je}, re and rc.

2.5.3. Decomposition of ECL dela

From Eq.(2.21) we see that the switching delay for a single one-input ECL gate can depend on various device parameters (SPICE parameters) and circuit parameters. As expected, to come up with just *one* exact closed-form expression of delay as a function of the 10 parameters listed above can be extremely difficult. In this thesis, the problem is simplified based on the technique of *divide and conquer*. By divide and conquer, we mean that the delay can be decomposed into separate stages. Each stage is marked by its own delay which constitutes a certain portion of the total delay. The key is that the delay function for each stage can be shown to depend on a few parameters only. Therefore, it is much easier to track down the delay function for each stage. However, it should be noted here that each stage is not completely independent of other stages. In other words, some overlap exists between the end of the switching waveform of a particular stage and the beginning of the

waveform of next stage. Moreover, some parameters may be common to the delay functions of more than just one stage. As a result, some approximations may have to be made as the analysis proceeds.

To start the decomposition, the total delay (τ_d) can be written as

$$\tau_d \approx \tau_{in} + \tau_{ext} \tag{2.22}$$

where τ_{in} stands for the **intrinsic delay**, and τ_{ext} stands for the **extrinsic delay**.

Further decomposition can be done to the extrinsic delay.

$$\tau_{ext} \approx \tau_{IV} + \tau_{buf} \tag{2.23}$$

where τ_{IV} stands for the I-V conversion delay, and τ_{buf} stands for the buffer (emitter follower) delay. The derivation of intrinsic delay will be presented in the next chapter.

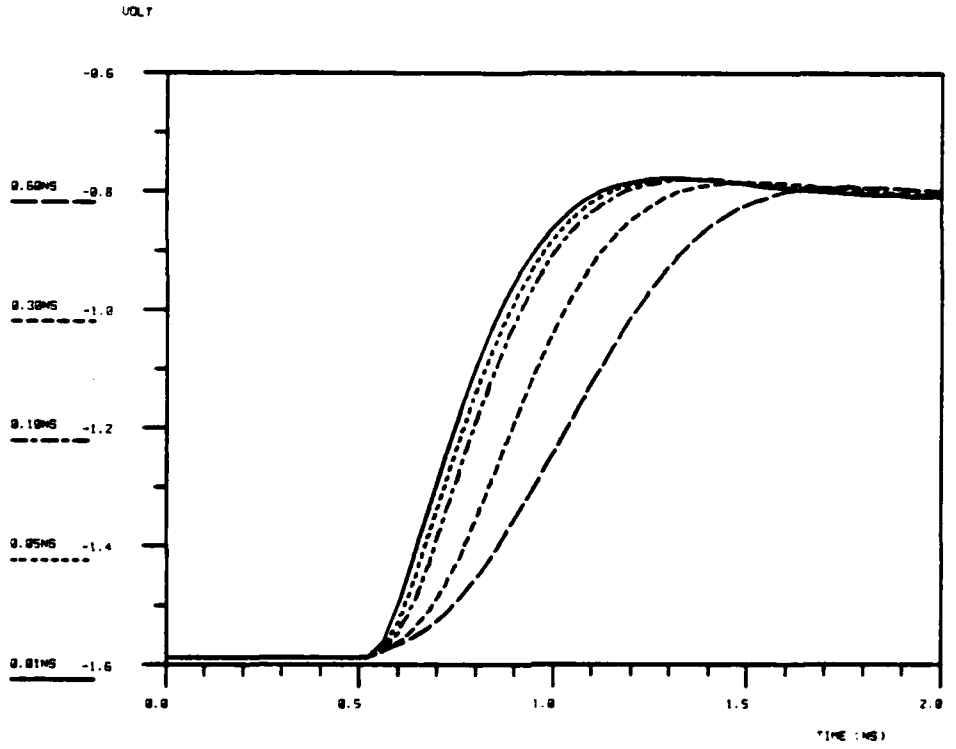

Figure 2.10 SPICE generated output at V2 (circuit shown in Fig.2.8) by varying Tf

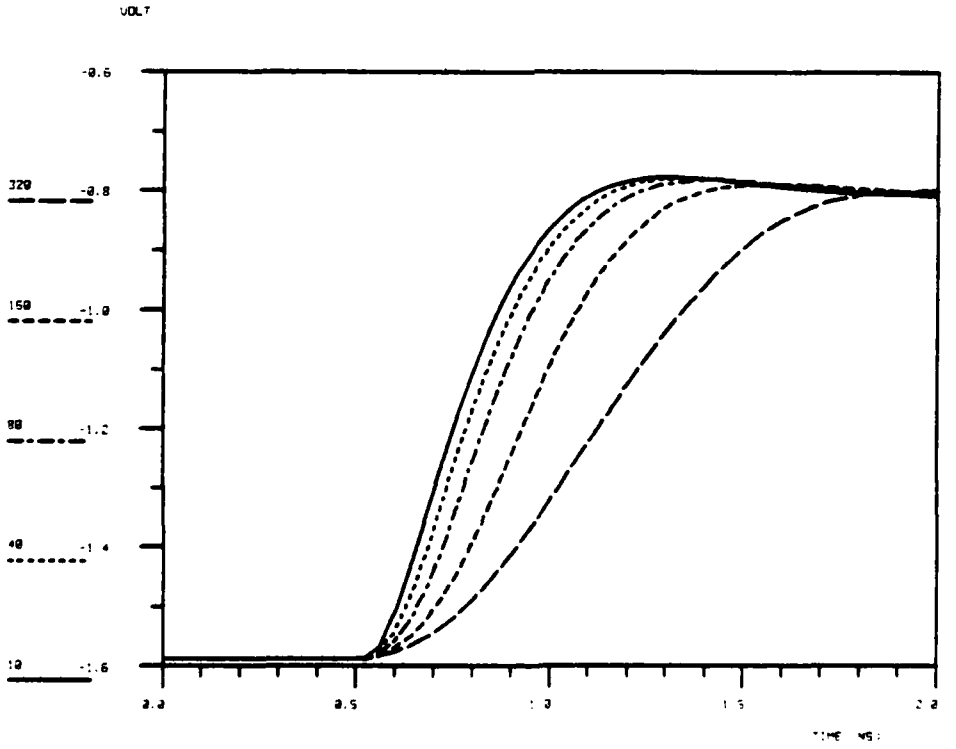

Figure 2.11 SPICE generated output at V2 (circuit shown in Fig.2.8) by varying rb

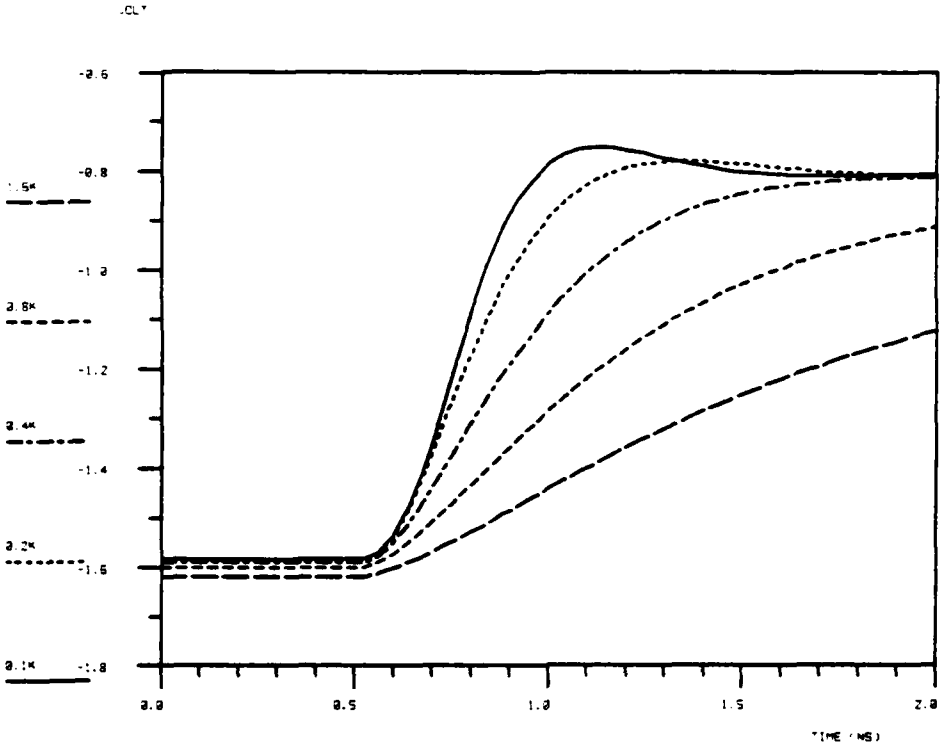

Figure 2.12 SPICE generated output at V2 (circuit shown in Fig.2.8) by varying Rc

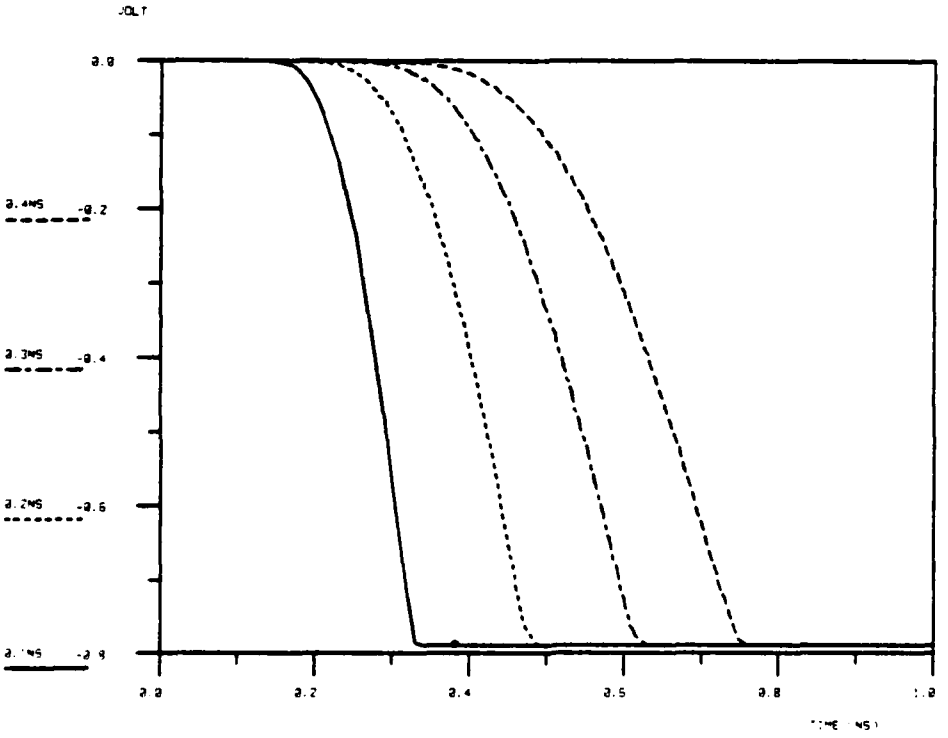

Figure 2.13 SPICE generated output at V2 (circuit shown in Fig.2.8) by varying Tslew

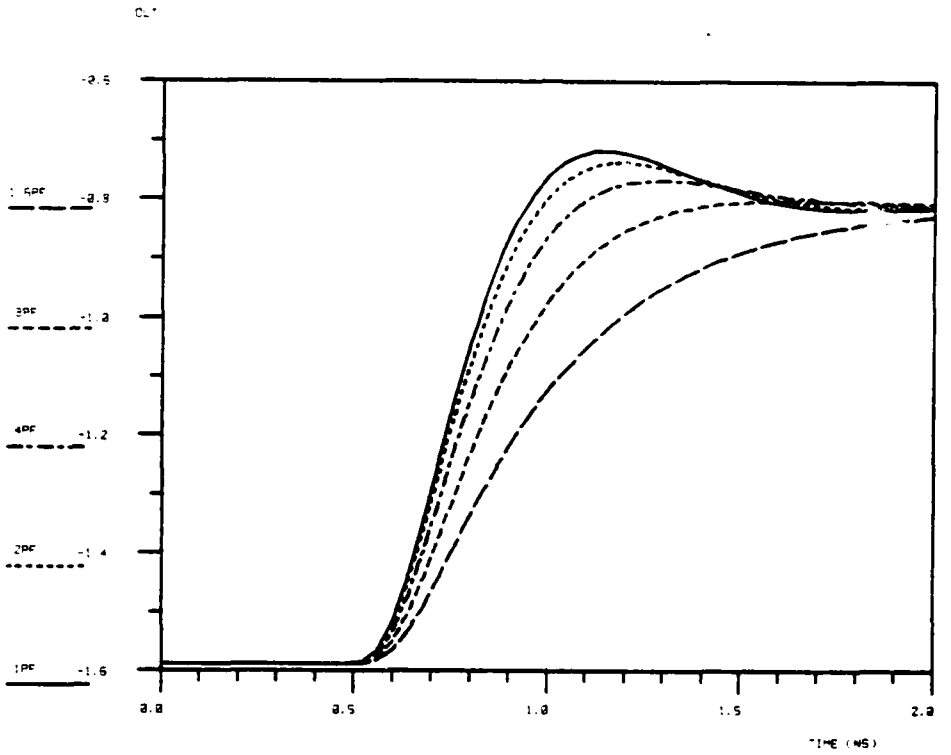

Figure 2.14 SPICE generated output at V2 (circuit shown in Fig.2.8) by varying Cjc

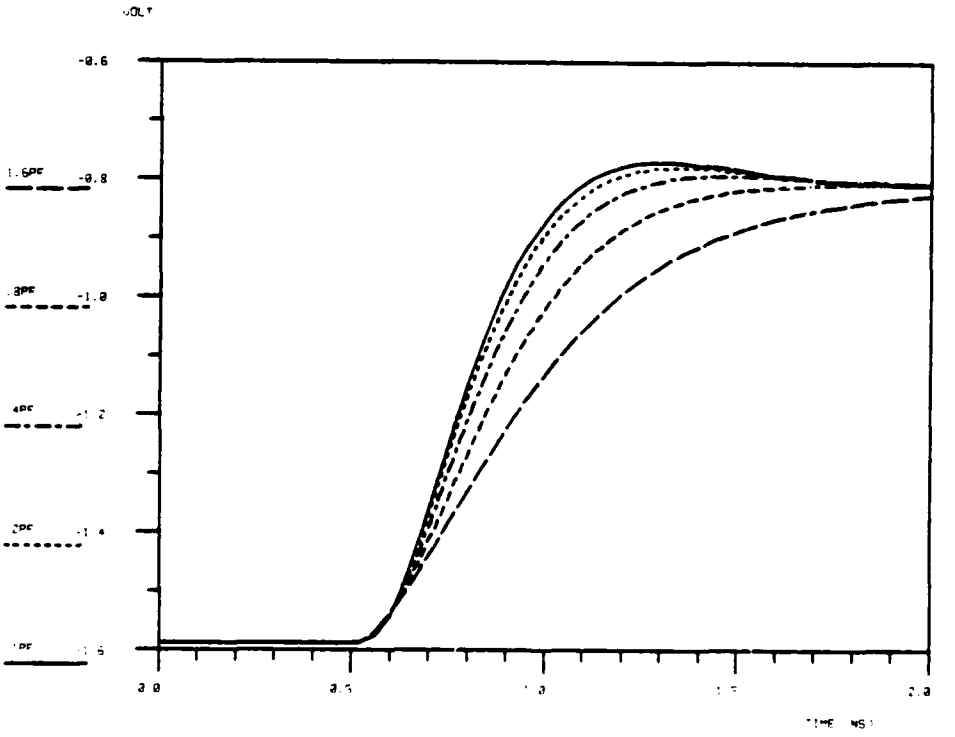

Figure 2.15 SPICE generated output at V2 (circuit shown in Fig.2.8) by varying Cccs

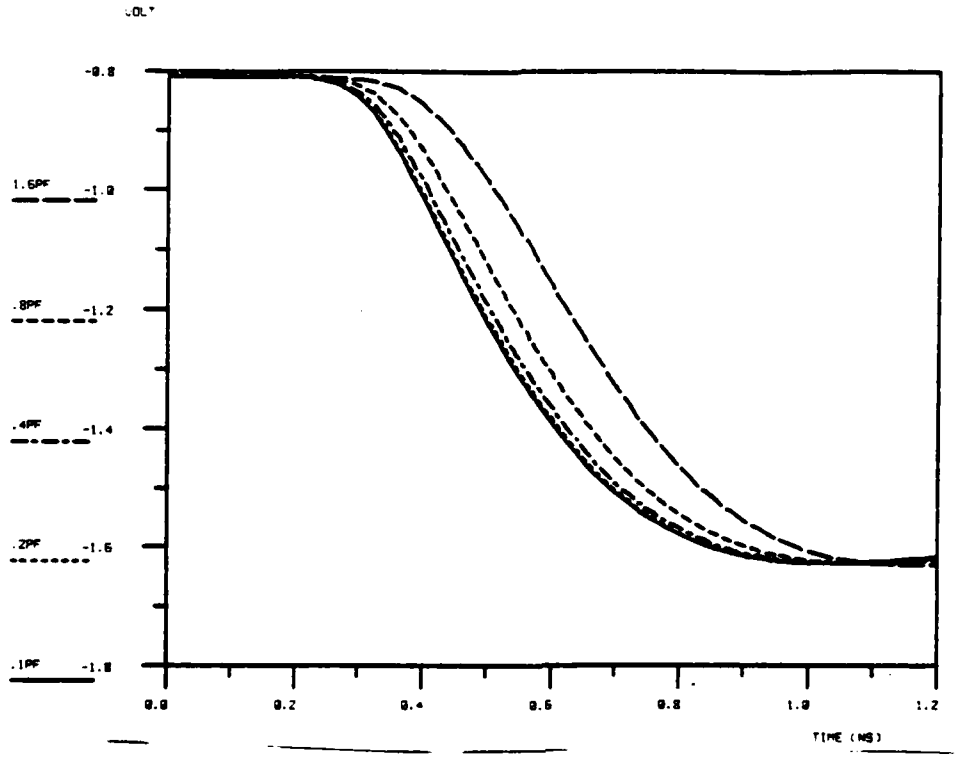

Figure 2.16 SPICE generated output at V2 (circuit shown in Fig.2.8) by varying Croot

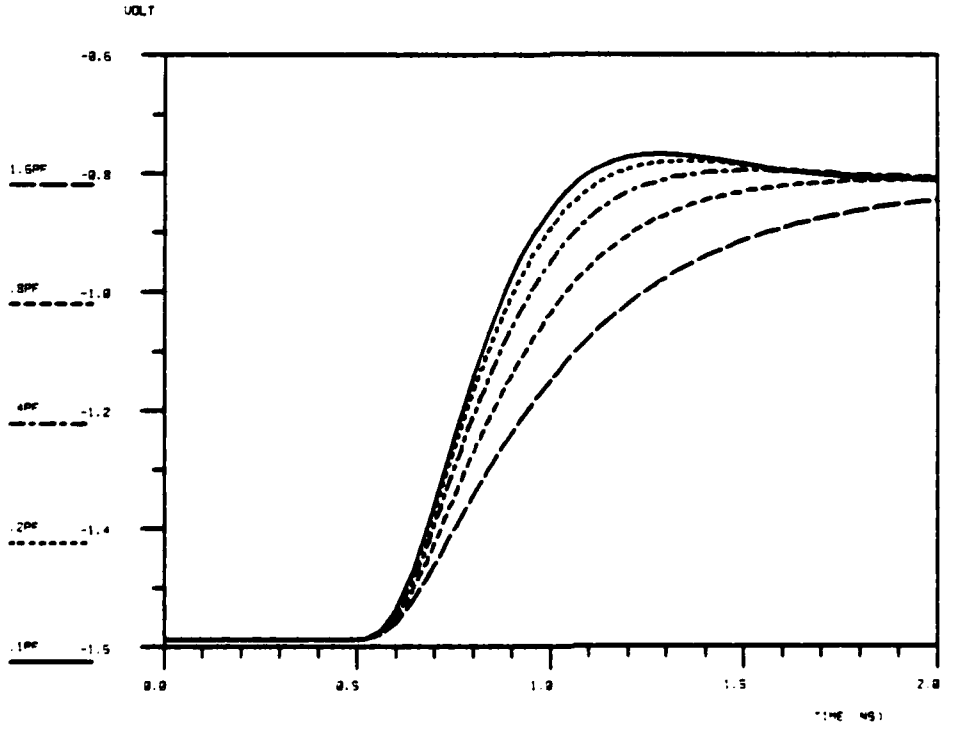

Figure 2.17 SPICE generated output at V2 (circuit shown in Fig.2.8) by varying Cjcf

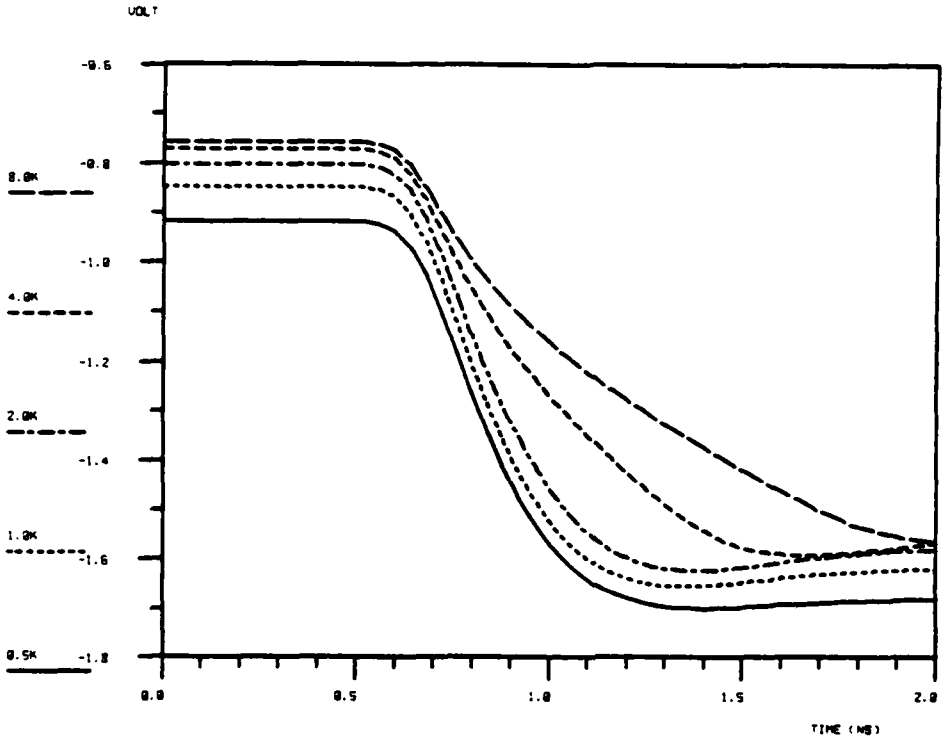

Figure 2.18 SPICE generated output at V2 (circuit shown in Fig.2.8) by varying Rf

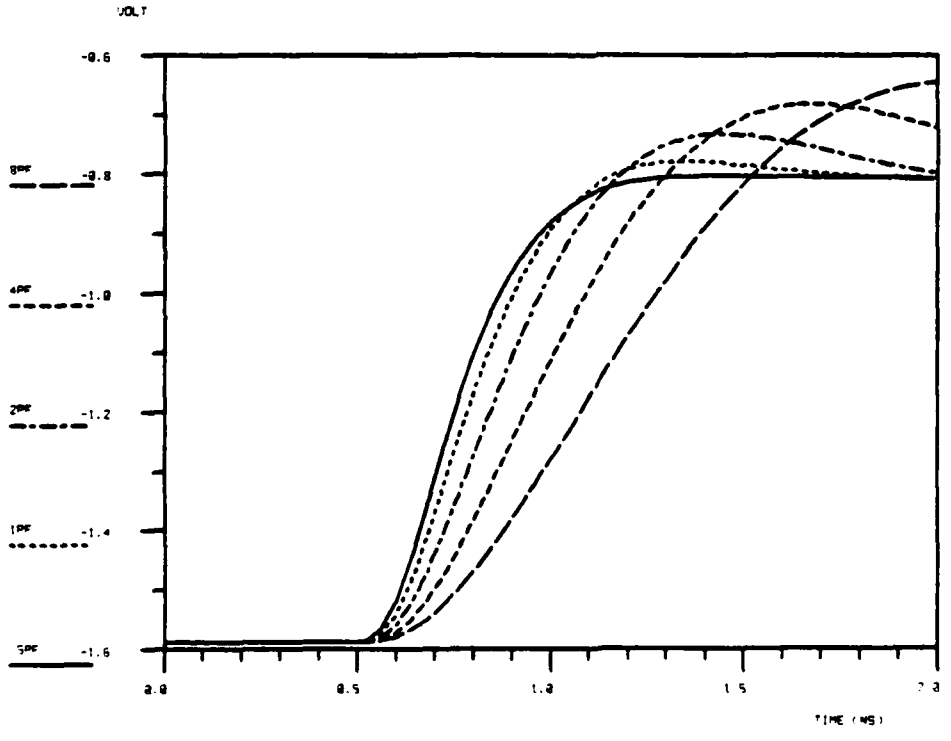

Figure 2.19 SPICE generated output at V2 (circuit shown in Fig.2.8) by varying Cload

CHAPTER 3

INTRINSIC DELAY OF ECL CIRCUITS

3.1. Introduction

From the previous chapter, a firstlook at the delay reveals that the delay function can be quite complex. The number of parameters in Eq.(2.21) are too many to be efficiently tackled. However, by decomposing the total delay into different stages, one can show that the delay function of each stage can be much simpler. The first stage that will be focused here is *intrinsic delay*.

τ_{in} , the intrinsic delay, contributes a significant portion to the total delay. Intrinsic delay is the time needed to turn on or turn off a transistor. For the particular applications where speed is of utmost importance, τ_{in} becomes the sole limitation to the performance. Therefore, it is crucial to be able to predict the intrinsic delay accurately. In fact, it will be shown in this chapter that by some model analysis, analytical expressions for τ_{in} can be derived. The expressions include the effects of input slew rate, T_{slew} .

Before we proceed, we need to establish a suitable delay definition. The propagation delay is defined as the time interval between the crossing of the *threshold level* of the input transition and the crossing of the same *threshold level* of the ensuing transition at the output. For MOS technology, the dc unity gain points provide good threshold levels. For ECL circuits, the midpoint of the transition is a natural threshold level. With this delay definition established and in view of Eq.(2.8), we are ready to give a new definition to intrinsic delay of ECL circuits.

DEFINITION: Intrinsic delay is the time for the mechanism of extracting or injecting *half* of the total stored excess minority charges, Q_f , from the base of the "ON" transistor of the differential pair.

3.2. Ideal intrinsic delay

For a single-input, one-sided (nonsymmetrical) ECL gate, if there is *no* capacitive loading, C_{root}, associated with the current source, the intrinsic delay for this gate will be **ideal**. Strictly speaking, C_{root} always exists at the root of a differential pair. We begin our analysis with the ideal intrinsic delay by ignoring C_{root}. Later, we include C_{root} in our analysis of nonideal intrinsic delay.

To isolate τ_{in} from the total delay, we can eliminate all the parasitic junction capacitances from the differential pair transistors. Based on the forward active model that we discussed in Chapter 2 (see Fig. 2.5), a first-order model is drawn for the analysis of intrinsic delay in Fig. 3.1.

The input at B1 is driven by a voltage *step* between the two dc levels of the circuit (-0.9 V and -1.7 V). For the sake of our analysis, a dc current source of 4 mA is connected at the common

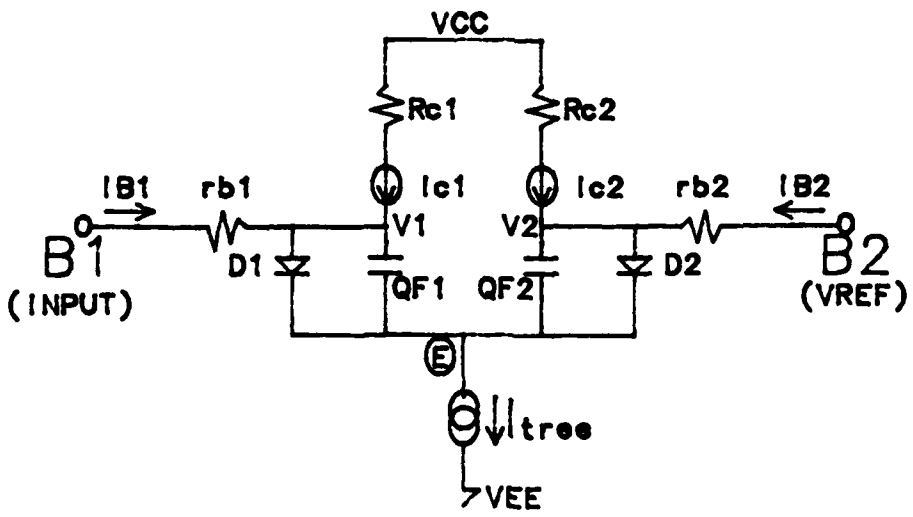

Figure 3.1 Model for intrinsic delay

node, E. For an output swing of ϕ, Rc1 and Rc2 are set to 200 ohms. The base currents I_{B1} and I_{B2} (with the drawn directions) represent forced currents from "sources" that will turn off and on the devices. From Eq. 2.16, we see that Q_{BEON} can be represented by a voltage-dependent nonlinear diffusion capacitor.

$$C_{BEON} = C_{dif} = \tau_f g_m \tag{3.1}$$

where g_m is a function of V_{BE}, and we know that

$$i(t) = \frac{C(V)dV}{dt} \tag{3.2}$$

Rearranging and integrating Eq.(3.2) results in

$$\int^{T} i(t)dt = \int^{V} C(V)dV \tag{3.3}$$

If i(t) can be approximated as a constant, i_{avg}, Eq.(3.3) can be written as

$$T = \frac{\int^{V} C(V)dV}{i_{avg}} \tag{3.4}$$

where T is the time it takes to change the voltage across the capacitor by an amount of V, and $\int^{V} C(V)dV$ is the change of charges corresponding to the change of voltage, V. From our definition of intrinsic delay, half of the total charges, Q_f, needs to be removed. Since

$$Q_f = \tau_f I_{tree} \tag{3.5}$$

$$\tau_{in} = \frac{1}{2}\frac{\tau_f I_{tree}}{i_{avg}} \tag{3.6}$$

Therefore, from the equation above, we see that in order to determine τ_{in}, i_{avg} must be known. Referring to Fig. 3.1, since I_{tree} equals the sum of I_{C1} and I_{C2}, an important observation from Kirchoff's current law is that

$$I_{B1} + I_{B2} = 0 \tag{3.7}$$

For a falling input step from -0.9 V down to -1.7 V at node B1, and a fixed VRS of -1.3 V at node B2, Eq.(3.7) can be satisfied only if

$$V_1 = V_2 = -1.5V \tag{3.8}$$

Due to the clamping effects of both D1 and D2, V_E will have a step drop of $\frac{3}{4}\phi$, or from -1.7 V down to -2.3 V. For a rising step from -1.7 V up to -0.9 V, the same approach can be applied except that V_E will have a step jump of *only* $\frac{1}{4}\phi$, or from -2.1 V up to -1.9 V. I_{B1} and I_{B2}, however, will not be different. From Eq.(3.8),

$$I_{B1} = -I_{B2} = \frac{V_{B1} - V_1}{rb} \tag{3.9}$$

or

$$I_{B1} = -\frac{0.2V}{rb} = -\frac{1}{4}\frac{\phi}{rb} \tag{3.10}$$

A SPICE simulation of I_{B1} and I_{B2} is shown in Fig. 3.2. The base resistance, rb, is 40 ohms. Note that currents remain fairly constant and have the value $\approx\frac{1}{4}\frac{\phi}{rb}$. Now, if one substitutes $-I_{B1}$ as i_{avg} into Eq.(3.6), we obtain an expression for ideal τ_{in}

$$\tau_{in\,(ideal)} = 2\frac{\tau_f\, I_{tree}\, rb}{\phi} \tag{3.11}$$

or

$$\tau_{in\,(ideal)} = \alpha\tau_f\, I_{tree}\, rb \tag{3.12}$$

From Eq.(3.11), if ϕ is 0.8 V, α is equal to 2.5. SPICE simulation shows $\tau_{in} \approx 2.6\tau_f\, I_{tree}\, rb$, with α of 2.6. Therefore, Eq.(3.11) is indeed quite an accurate expression for ideal intrinsic delay. It should be pointed out here that from the analysis above, one can show that for ideal intrinsic delay

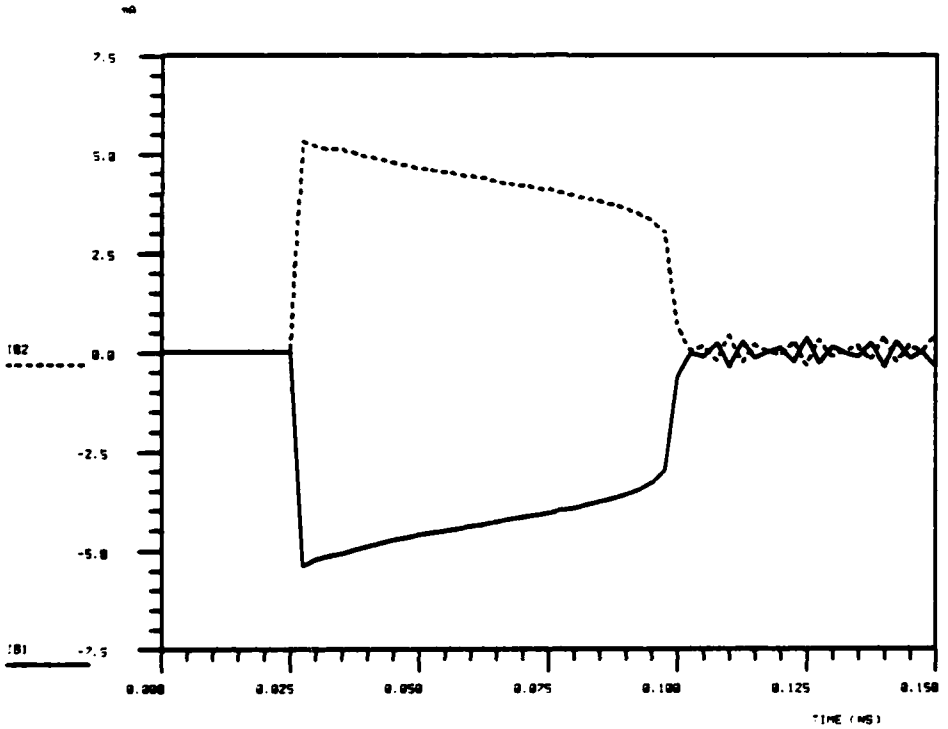

Figure 3.2 Discharging currents at the bases of the differential-pair transistors for intrinsic delay

$$\tau_{rise\,(ideal)} = \tau_{fall\,(ideal)} \tag{3.13}$$

Figure 3.3 shows an output of typical τ_{rise} and τ_{fall} waveforms of intrinsic delay. Figure 3.4 shows several comparisons of predicted and actual waveforms of τ_{in}. The values for rb, τ_f and I_{tree} are randomly chosen.

Finally, Eq.(3.11) can be written in a more compact way if we replace I_{tree} by $\frac{\phi}{Rc}$.

$$\tau_{in\,(ideal)} = 2\tau_f \frac{rb}{Rc} \tag{3.14}$$

Equation (3.14) provides an extremely simple *rule of thumb* for the computation of intrinsic delay.

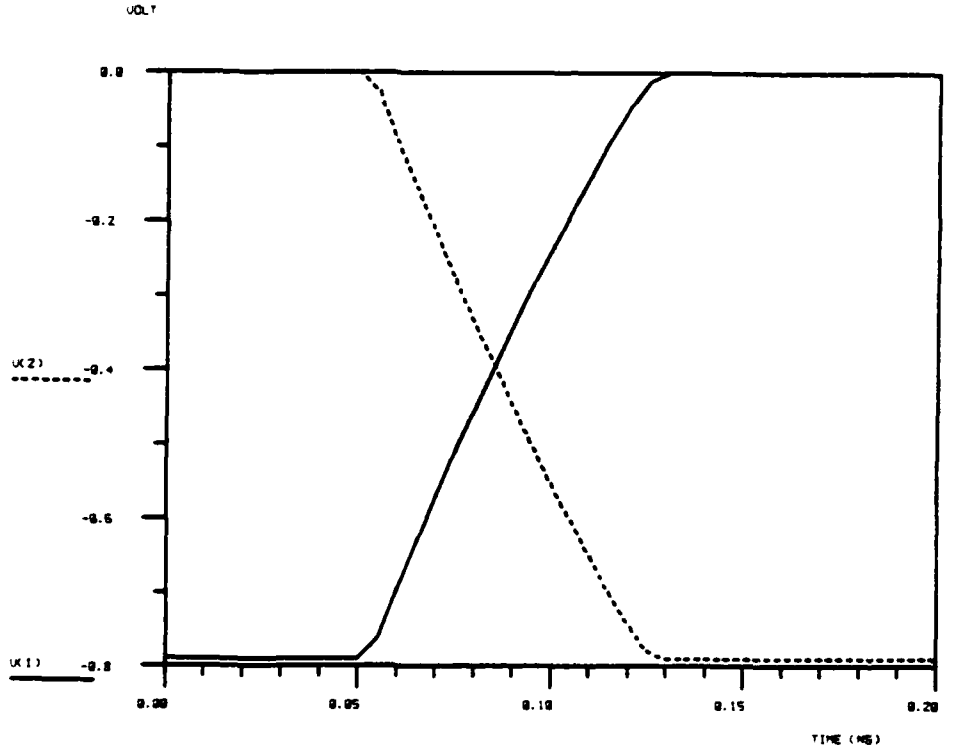

Figure 3.3 Waveforms of ideal intrinsic delay

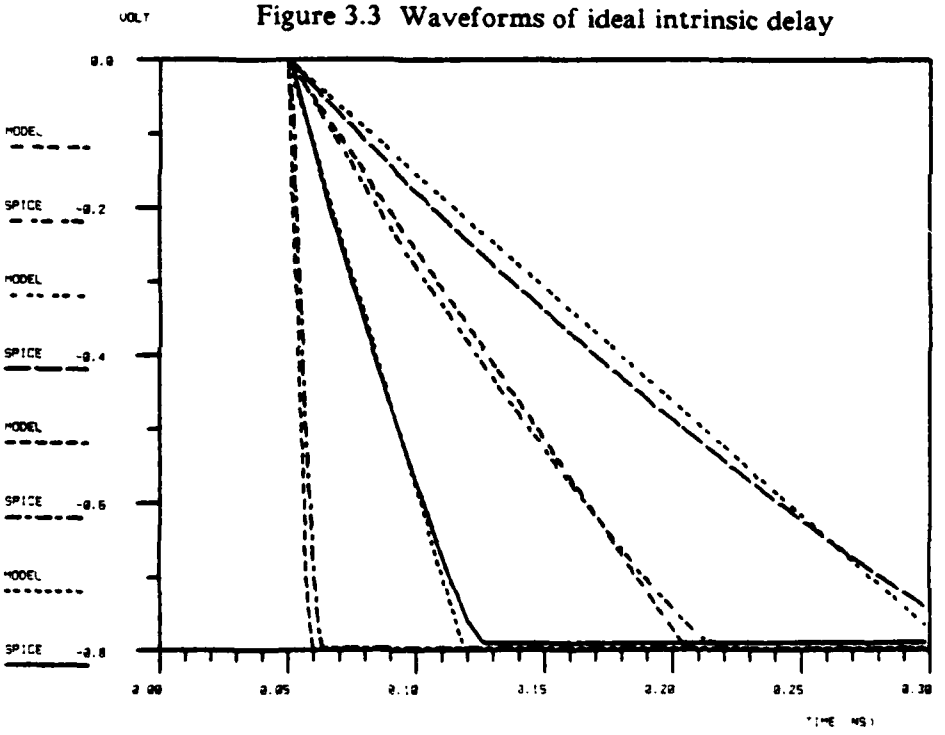

Figure 3.4 Comparisons of actual and predicted intrinsic delays

3.3. Nonideal intrinsic delay

From the last section, a very compact expression for τ_{in} is presented for the ideal case. As mentioned before, there is always a capacitance, C_{root}, associated with the current source. For a two-level or three-level ECL circuit, C_{root} is the capacitance at the collector of a differential pair transistor. In this section, the effects of C_{root} will be included in our analysis of intrinsic delay. Since the results will deviate somewhat from what we have obtained for the ideal case, the intrinsic delay (with the effects of C_{root} included) is described as being **nonideal**.

3.3.1. Rising step input

Consider the equivalent model (Fig. 3.5) with C_{root} included. Again, the input at B1 is driven by a voltage step between two dc levels (-0.9 V and -1.7 V). For a *rising step input*, V_E needs to

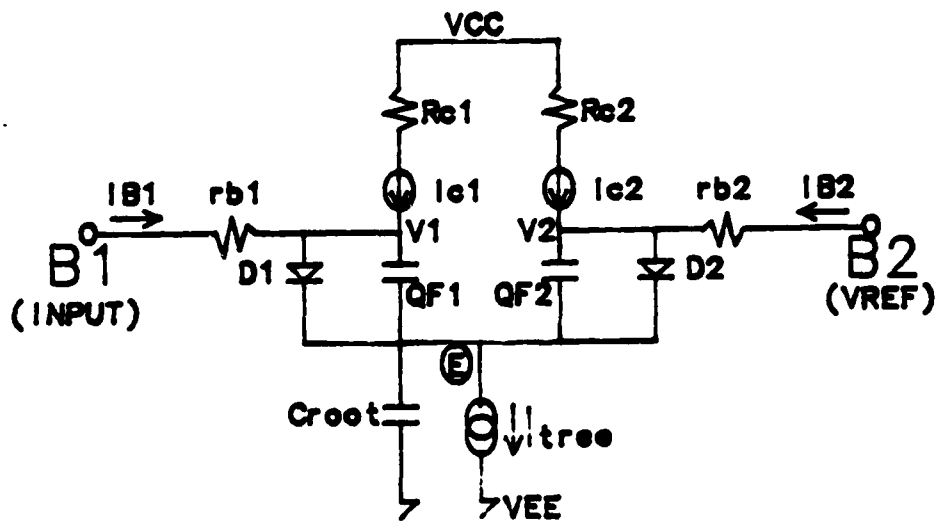

Fig. 3.5 Model for nonideal intrinsic delay

rise from -2.1 V to -1.9 V ($\frac{1}{4}\phi$). In other words, C_{root} needs to be charged up for a swing of $\frac{1}{4}\phi$. This, in addition to the ideal intrinsic delay, results in an extra delay. This charge-up process, however, is very fast. The reasons are twofold. First, the emitter follower (through the differential pair transistor) can provide very fast charge-up action. Second, the swing is small ($\approx 0.2V$). Therefore, this extra delay for a rising step input can be safely neglected. In fact, SPICE shows that this extra delay is less than 10% of the ideal intrinsic delay.

3.3.2. Falling step input

On the other hand, if the input at B1 is switching from high to low, C_{root} needs to be discharged for a much higher swing ($\frac{3}{4}\phi$). The discharging mechanism, comparatively, is also much slower. Therefore, one cannot neglect this extra delay. Moreover, for non-ideal intrinsic delay

$$\tau_{rise} \neq \tau_{fall} \tag{3.15}$$

Figure 3.6 shows the drastic shifts of τ_{rise} and τ_{fall} from the ideal intrinsic delay waveforms. Qualitatively, the effects of C_{root} on a falling input at B1 are as follows.

1. Since V_E is falling slowly and V_1 is clamped at higher voltage, more I_{B1} is available to discharge Q_{F1}. Therefore, V_1 rises considerably faster than it would for the ideal case.

2. Since V_E is falling slowly, V_2 stays quite high and less I_{B2} is available to charge Q_{F2}. Therefore, V_2 falls considerably slower than it would for the ideal case.

Therefore, to derive quantitative expressions for τ_{rise} and τ_{fall}, I_{B1} and I_{B2} must be known. Moreover, in addition to the charge storage in the base, charges are also stored in C_{root} as Q_{root}. From Eq.(2.12)

$$Ceq_{root} = K_{eq} C_{root} \tag{3.16}$$

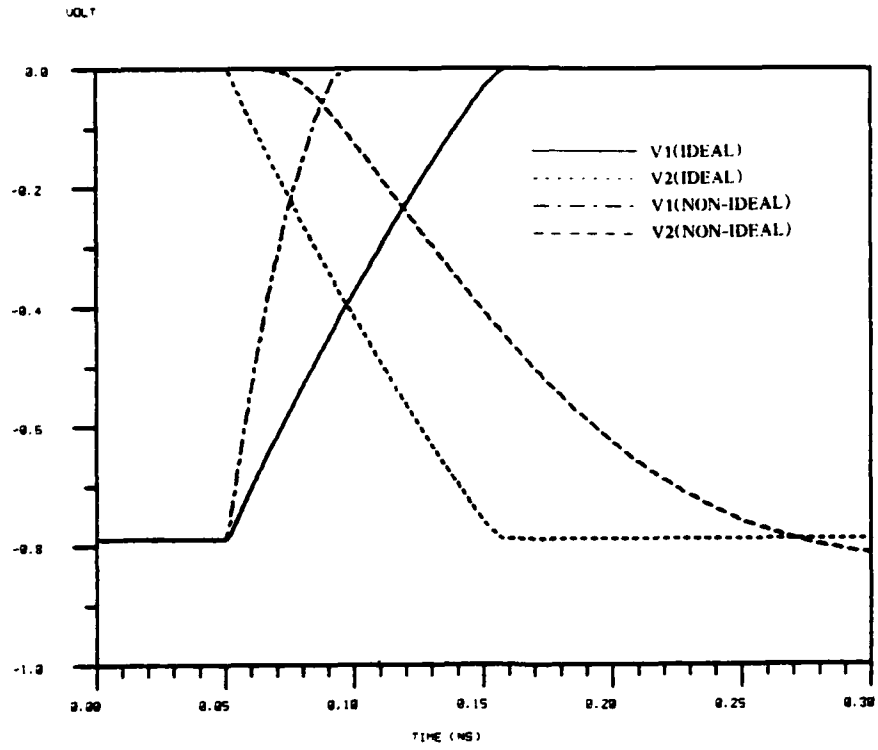

Figure 3.6 Shifts of waveforms for nonideal delay from ideal case

where K_{eq} can be evaluated readily by Eq.(2.13) once the swing across C_{root} is known ($\frac{3}{4}\phi$). From now on, we will assume that all the voltage-dependent capacitors are replaced by their equivalent constant capacitors.

$$Q_{root} = C_{root}\frac{3}{4}\phi \tag{3.17}$$

Note that as soon as the input falls, V_1 and V_E are fixed. As a result, a *peak* current, I_{peak}, flows out of B1 immediately. It will discharge *both* Q_{F1} and Q_{root} simultaneously. As Q_{F1} and Q_{root} are being discharged, V_1 and V_E will drop. This, in turn, causes a drop of discharging current from its peak value of I_{peak}. The discharging current will continue to drop until C_{root} is discharged for a full $\frac{3}{4}\phi$. Taking $\frac{1}{2}$ of I_{peak} is a valid average for this falling current

$$I_{root} = \frac{1}{2}I_{peak} = \frac{1}{2}\frac{\phi}{rb} \tag{3.18}$$

where I_{root} stands for the average discharging current for C_{root}. Soon after C_{root} has been

discharged fully and if Q_{F1} still needs to be charged further, the discharging current then will be

$$I_{qf} = \frac{1}{4}\frac{\phi}{rb} \tag{3.19}$$

where I_{qf} stands for the discharging current for Q_{F1}. The notations used may be quite misleading, since Q_{F1} is also being discharged by I_{root} as well.

Now that we know Q_{root}, I_{root} and I_{qf}, we can use Eq.(3.6) to derive expressions for τ_{rise} and τ_{fall} for nonideal intrinsic delay. If $\frac{1}{2}Q_{F1} \leqslant Q_{root}$ (large C_{root}), half of the stored minority charges will be discharged completely by I_{root}, or

$$\tau_{rise} = \frac{\frac{1}{2}\tau_f I_{tree}}{I_{root}} \tag{3.20}$$

Substituting Eq.(3.18) for I_{tree}, we obtain

$$\tau_{\text{rise}} = \tau_{\text{f}} \frac{\text{rb}}{\text{Rc}} \qquad \text{if} \qquad \frac{1}{2}\text{Q}_{\text{F1}} \leqslant \text{Q}_{\text{root}} \tag{3.21}$$

Equation (3.21) is a compact expression which implies that the *absolute limit* of the fastest switching intrinsic delay is the product of τ_f with $\frac{rb}{Rc}$. Comparing this result with Eq.(3.14), we see that for large C_{root}, τ_{rise} (for a falling input) can be as small as *half* of the ideal intrinsic delay. For the case when $\frac{1}{2}Q_{F1} \geqslant Q_{root}$ (small C_{root}),

$$\tau_{rise} = \frac{\frac{1}{2}\tau_f I_{tree} - Q_{root}}{I_{qf}} + \frac{Q_{root}}{I_{root}} \tag{3.22}$$

Substituting the expressions for I_{tree} and I_{qf} into Eq.(3.22) and simplifying, we obtain

$$\tau_{rise} = 2\tau_f \frac{rb}{Rc} - \frac{Q_{root}}{\phi}(2rb) \tag{3.23}$$

Substituting Eq.(3.17) for Q_{root}, we have

$$\tau_{\text{rise}} = 2\tau_{\text{f}} \frac{\text{rb}}{\text{Rc}} - \frac{3}{2}\text{C}_{\text{root}}\,\text{rb} \qquad \text{if} \qquad \frac{1}{2}\text{Q}_{\text{F1}} \geq \text{Q}_{\text{root}} \tag{3.24}$$

Note that the first component in Eq.(3.24) is equal to the ideal intrinsic delay, as it should.

Again, Eq.(3.24) is a compact expression, and it implies that for small C_{root}, τ_{rise} is reduced from $\tau_{in\,(ideal)}$ by a value that is linearly dependent on C_{root} and rb. If C_{root} =0, Eq.(3.24) reduces to the ideal intrinsic delay.

Equations (3.21) and (3.24) provide a compact solution of τ_{rise} when the input is falling from high to low and C_{root} is included. The validities of these two expressions are well supported by the results of simulation using SPICE.

The expression for τ_{fall} can be written as

$$\tau_{fall} = \tau_{in\,(ideal)} + \tau_{extra} \tag{3.25}$$

where $\tau_{in\,(ideal)}$ stands for the ideal intrinsic delay and τ_{extra} stands for the extra time it takes to discharge C_{root}. To discharge C_{root} for $\frac{3}{4}\phi$ from its initial -1.7 V, an extra time is needed.

$$\tau_{extra} = \frac{Q_{root}}{I_{root}} \tag{3.26}$$

However, a full discharge of $\frac{3}{4}\phi$ is not required before the charging current starts to flow into B2. Actually, the charging current can be assumed to flow when C_{root} is discharged halfway. Therefore, a factor of $\frac{1}{2}$ should be included in Eq.(3.17). Combining Eq.(3.26) with Eq.(3.25) and substituting Eq.(3.18) for I_{root}, we obtain

$$\tau_{\text{fall}} = 2\tau_{\text{f}} \frac{\text{rb}}{\text{Rc}} + \frac{3}{4}\text{C}_{\text{root}}\,\text{rb} \tag{3.27}$$

Again, Eq.(3.27) reduces to the ideal intrinsic delay when C_{root} =0.

3.4. Input slew rate

So far, our analysis was based on input that is an ideal step function. In reality, different *input slew rates*, T_{slew} are encountered. It will be shown in this section that to account for the effects of T_{slew}, only minor adjustments to our already obtained results are needed.

If we sum the voltages around the loop consisting of the two input sources and the two base-emitter junctions, we obtain

$$V_{i1} - V_{be1} + V_{be2} - V_{i2} = 0 \tag{3.28}$$

From the ideal diode equation, $V_{be1} = V_T ln(\frac{I_e}{I_S})$, and defining V_{id} as $V_{i1} - V_{i2}$, we have

$$V_{id} = V_T \ln(\frac{I_{c1}}{I_{c2}}) \tag{3.29}$$

With V_{id} = 60 mV, $I_{c1} = 10I_{c2}$. With V_{id} = -60 mV, $I_{c1} = 0.1I_{c2}$. Therefore, the transition height, V_{height}, is approximately 120 mV, and *centered* at VRS.

In Fig. 3.7, we define $T_{slew} = t_2 - t_1$ as a measure of the slew rate of the input signal. V_{th} and t_{th} are the input threshold voltage and its corresponding threshold crossing time, respectively. The output waveforms are defined by t_1' and t_2'. Note that the transition from one logic state to the other is centered at the reference voltage VRS, and obviously, VRS = V_{th}. Hence, $t_1' = t_{th}$. From our delay definition for ECL logic,

$$\tau_d = t_2' - t_1' \tag{3.30}$$

Therefore, given T_{slew}, we can obtain t_1' directly. From our delay operator, τ_d can be calculated. We should be able then to approximate the output waveform by a straight line with slope defined by t_1' and t_2'.

Yet another adjustment should be taken into account. Our delay operator derived so far assumes an ideal input step, or a transition with infinite slope. In other words, it takes no time for the input waveform to cross the transition height, V_{height}. In reality, time is needed for crossing the

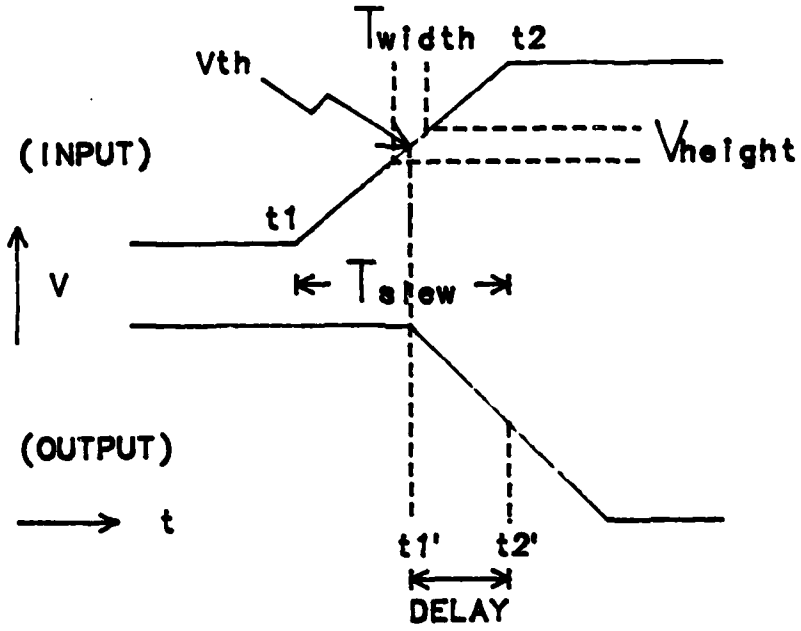

Figure 3.7 Threshold crossings for input and output

transition height. It is called the transition width, τ_{width}. It can be easily shown that

$$\tau_{width} = \frac{V_{height}}{\phi} T_{slew} \tag{3.31}$$

or,

$$\tau_{width} \approx 0.15 T_{slew} \tag{3.32}$$

3.5. Summary

It is shown in this chapter that the intrinsic delay function can be expressed as

$$\tau_{in} \approx f_{in}(rb, \tau_f, Rc, C_{root}, T_{slew})_{first-order} \tag{3.33}$$

Several important comments relating to the expression above deserve to be pointed out here. First, from our basic definition of *intrinsic delay*, we see that the delay is related to the number of charges stored in the base region. These charges, in turn, have a linear dependence on the *power (current)* of the device. In fact, they are related by an important device parameter, τ_f (Eq.2.8). Thus, we see that the intrinsic delay is directly affected by τ_f. Since τ_f is controlled by the processing (fabrication) of the device, it poses a *fundermental* limit to the performance of ECL circuits. Or, in other words, ECL circuits are inherently τ_f *–limited*. Second, the rate of extracting, or injecting these storage charges depends on the the amount of discharging, or charging current at the base. The base resistance, r_b, is another important device parameter that will affect these currents. Therefore, one would like to minimize r_b by keeping the transistor size as small as possible to reduce the intrinsic delay. Unfortunately, there exists an important trade-off to the design of transistor size through the circuit parameter, R_c. This topic will be discussed in the next chapter.

The key expressions derived here are Eq.(3.14), Eq.(3.21), Eq.(3.24), Eq.(3.27) and Eq.(3.32). They can be rearranged and summarized as follows.

LOGIC GATE: NON-SYMMETRICAL (ONE-SIDED) ECL GATE

DELAY: INTRINSIC DELAY

A) INPUT FROM LOW TO HIGH

$$\tau_{rise} = \tau_{fall} = 2\tau_f \frac{rb}{Rc} + 0.15T_{slew}$$

B) INPUT FROM HIGH TO LOW

$$\tau_{rise} = \tau_f \frac{rb}{Rc} + 0.15T_{slew} \qquad \text{if} \qquad \frac{1}{2}Q_{F1} \leq Q_{root}$$

$$= 2\tau_f \frac{rb}{Rc} - \frac{3}{2}C_{root}\, rb + 0.15T_{slew} \qquad \text{if} \qquad \frac{1}{2}Q_{F1} > Q_{root}$$

$$\tau_{fall} = 2\tau_f \frac{rb}{Rc} + \frac{3}{4}C_{root}\, rb + 0.15T_{slew}$$

CHAPTER 4

EXTRINSIC DELAY OF ECL CIRCUITS

4.1. Introduction

In Chapter 3, important expressions describing the intrinsic delay, τ_{in}, are derived, and are shown to depend on several parameters, namely, rb, τ_f, Rc, C_{root} and T_{slew}. One would like to design Rc as large as possible to minimize the intrinsic delay. However, it will be shown in this chapter that a larger value of Rc leads to an increase of the *extrinsic delay*, τ_{ext}.

Extrinsic delay is important because it strongly affects the performance of ECL circuits, especially when the circuits operate under *low power*. It will be shown to depend on the parasitic capacitances associated with the transistors as well as the interconnection capacitances. We can define the extrinsic delay as follows.

DEFINITION: Extrinsic delay is the time for the mechanism of charging or discharging all the associated capacitances through half a voltage swing ($\frac{1}{2}\phi$) at the output node.

Before we proceed with our discussion on extrinsic delay, we will decompose it into *I-V conversion* delay and *emitter follower* delay. However, it should be understood that this decomposition is only to facilitate our discussion. In reality, one cannot distinguish one from the other.

4.2. I-V conversion delay

The delay associated with converting the current back to voltage by means of a pull-up resistor can be modeled by a simple RC time constant at the collector of the transistor. This simple RC model is illustrated in Fig. 4.1, where node 1 is connected to both the collector of the differential pair transistor and the base of the emitter follower. For the time being, the emitter follower is

ignored. The pull-down current source, $Ic(t)$, can be modeled by a straight line with slope determined by the intrinsic delay. From basic circuit analysis, the exact solution of the time-dependent waveform at node 1 for the RC model with input ramp functions is

$$v(t) = \frac{I_{tree} Rc^2 Ct}{T_{end}}\left(1 - e^{\frac{-t}{RcCt}}\right) - \frac{I_{tree} Rc}{T_{end}} \tag{4.1}$$

$$- \frac{I_{tree} Rc^2 Ct}{T_{end}}\left(1 - e^{-\frac{(t - T_{end})}{RcCt}}\right) + \frac{I_{tree} Rc}{T_{tree}}(t - T_{end})$$

T_{end} is the time where the ramp function flattens out. Note that iteration on Eq.(4.1) is necessary to obtain the time for any specified v.

For the output voltage to change half of the output swing (ϕ), a simple approximation to Eq.(4.1) can be obtained by replacing the ramp-function current source by an ideal step current source, as shown in Fig. 4.1. The solution then can be obtained by a simple RC analysis. For charge-up, the voltage as a function of time is given by

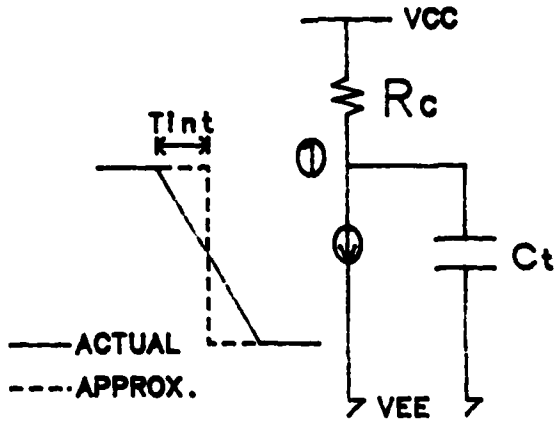

Figure 4.1 RC equivalent circuit model

$$V_1(t) = -I_{tree} R_c e^{\frac{-t}{R_c C_t}} \tag{4.2}$$

For discharge, the voltage as a function of time is given by

$$V_1(t) = -I_{tree} R_c (1 - e^{\frac{-t}{R_c C_t}}) \tag{4.3}$$

Let us denote the time for output to change half of ϕ as the delay constant, τ_{RC}. It is equal to

$$\tau_{RC} = R_c C_t \ln(\frac{1}{2}) \tag{4.4}$$

or,

$$\tau_{RC} = 0.693 R_c C_t \tag{4.5}$$

The results evaluated by Eq.(4.5) and Eq.(4.1) for any given R_c and C_t can be shown to be quite compatible (with less than 2% error).

The total capacitance at node 1 is a simple sum of the parasitic capacitance of various elements connected to the node. Again, from Eq.(2.12), the voltage-dependent pn junction capacitors can be replaced by constant voltage-independent capacitors. K_{eq} for each junction capacitor can be readily computed since the voltage swing across the capacitor is ϕ. From this point on, we will assume that every junction capacitor is replaced by a constant capacitor. Therefore,

$$\tau_{RC} = 0.693 R_c (C_{ccs} + C_{jc} + C_{jc} f) \tag{4.6}$$

where $C_{jc} f$ is the base-collector capacitance of the emitter follower. If the base-collector capacitance, C_{jc}, of the differential transistor provides coupling between the input and output, Eq.(4.6) should be modified to

$$\tau_{RC} = 0.693 R_c (C_{ccs} + 1.8 C_{jc} + C_{jc} f) \tag{4.7}$$

where the factor 1.8 is an empirical number observed from SPICE results. It is introduced to account for the *Miller effect*.

4.3. Emitter follower delay

The *emitter follower delay* is more difficult to be analyzed. Its main difficulty arises from the fact that it is strongly tied to the I-V conversion delay. Moreover, its effects on τ_{rise} and τ_{fall} are quite different.

4.3.1. Emitter follower charge-up

A full consideration of the transistor model is necessary to our analysis of τ_{rise}. When the output in switching from low (-2ϕ) to high ($-\phi$), the emitter follower transistor is fully turned on to provide the neccessary *drive* to the output loads. Using the forward biased model for the emitter follower transistor, an equivalent circuit is drawn in Fig. 4.2.

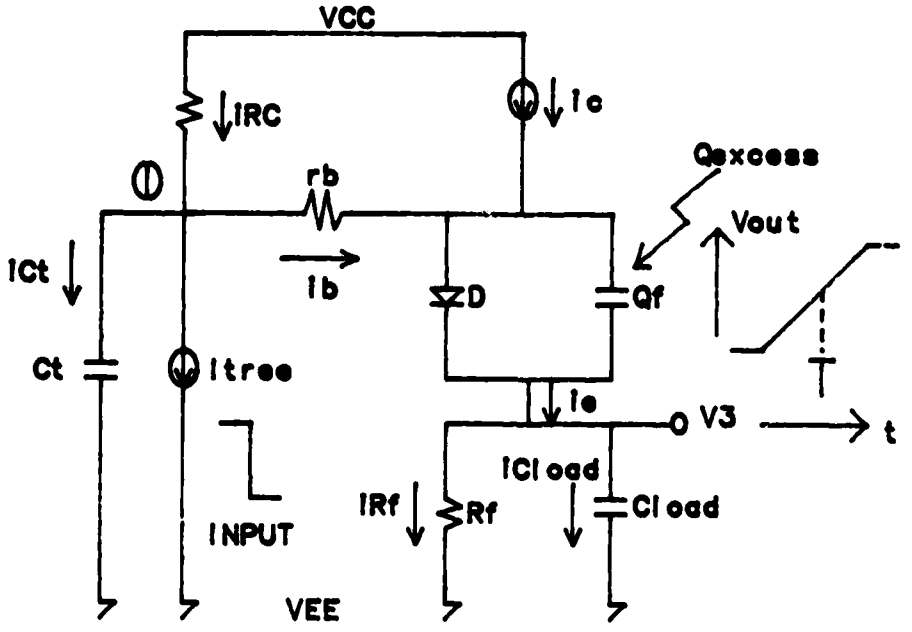

Figure 4.2 Equivalent circuit for emitter-follower action

Qualitatively, when the current is switched away, base node (node 1) is being pulled up by Rc. However, the output node (node 3) will not respond instantly because the voltage across C_{dif} cannot change instantly. Hence, an excess (transient) base current flows in to charge C_{dif} . These excess charges in the base are reflected as excess emitter current used to charge up the loads. Note that the collector is tied to the power supply. Thus, no current limitation is imposed on the emitter current.

Before we proceed with our quantitative analysis, an important point should be stressed. As described by Eq.(3.4), a key to our analysis is to determine the average transient current, i_{avg} , flowing into or out of every capacitor in question. As a result, every current described, unless stated otherwise, is considered to have a constant average value for the period of interest.

In Chapter 2 we introduced the charge-control model to describe the transient behaviors for a forward biased bipolar transistor. Equations (2.9), (2.10) and (2.12) are repeated here.

$$i_c(t) = \frac{Q_f(t)}{\tau_f} \tag{4.8}$$

$$i_b(t) = \frac{Q_f(t)}{\tau_{bf}} + \frac{dQ_f}{dt} \tag{4.9}$$

$$i_e(t) = \frac{Q_f(t)}{\tau_f} + \frac{Q_f(t)}{\tau_{bf}} + \frac{dQ_f}{dt} \tag{4.10}$$

During the period of charge-up, excess charges are injected by excess base current into the base region. They are stored as *temporary* excess minority carriers, Q_{excess} . Neglecting the steady-state term in Eq.(4.9) and replacing $i_b(t)$ by an average value, i_b , one obtains

$$i_b t = Q_{excess} \tag{4.11}$$

Since $i_b(t)$ can be approximated by a linearly increasing function for the period of interest (τ_{rise}), the average value of i_b is obtained when t is equal to $\frac{T}{2}$ (T is the period of interest, see Fig.4.2).

Therefore,

$$\frac{i_b T}{2} = Q_{excess} \tag{4.12}$$

From Eq.(4.8) and Eq.(4.10), we have

$$i_c = \frac{i_b T}{2\tau_f} \tag{4.13}$$

$$i_e = \frac{i_b T}{2\tau_f} + i_b \tag{4.14}$$

or

$$i_e = i_b\left(\frac{T}{2\tau_f} + 1\right) \tag{4.15}$$

At the load, from Eq.(3.4), we can write

$$T = \frac{C_{load}\,\psi_e}{i_{Cload}} \tag{4.16}$$

where ψ_e stands for the total voltage change at the *emitter* of the emitter follower transistor (output) during the period of interest, T.

As output changes, the current through the loading resistor, R_f, also changes. However, to simplify our analysis, we assume this increase to be negligible. Later, we drop this approximation to account for the effect of R_f on the charge-up action. For the time being, we can write

$$i_e \approx i_{Cload} \tag{4.17}$$

Equating Eq.(4.14) and Eq.(4.17), one obtains

$$\frac{C_{load}\,\psi_e}{T} = \frac{i_b T}{2\tau_f} + i_b \tag{4.18}$$

Rearanging Eq.(4.18), we obtain a quadratic equation of T.

$$\frac{i_b}{2\tau_f}T^2 + i_b T - C_{load}\psi_e = 0 \tag{4.19}$$

From Fig.4.2, Kirchoff's current law at node 1 states ($I_{tree} = 0$)

$$i_b = i_{Rc} - i_{Ct} \tag{4.20}$$

Again from Eq.(3.4) we have

$$i_{Ct} = \frac{C_t \psi_b}{T} \tag{4.21}$$

where ψ_b stands for the voltage change at the base (node 1) of the emitter follower during the period of interest.

Substituting Eq.(4.20) and Eq.(4.21) into Eq.(4.19), we obtain

$$\frac{i_{Rc}}{2\tau_f}T^2 - (\frac{C_t \psi_b}{2\tau_f} - i_{Rc})T - (C_t \psi_b + C_{load}\psi_e) = 0 \tag{4.22}$$

which has a solution of

$$T = \frac{C_t \psi_b}{2i_{Rc}} - \tau_f + \frac{\tau_f}{i_{Rc}}\sqrt{(\frac{C_t \psi_b}{2\tau\tau_f})^2 + \frac{i_{Rc} C_t \psi_b}{\tau_f} + \frac{2i_{Rc} C_{load}\psi_e}{\tau_f} + i_{Rc}^2} \tag{4.23}$$

Equation (4.23) is an important expression relating T (period of interest) to several parameters including *both* C_{load} and C_t. Yet, i_{Rc}, ψ_b and ψ_e still need to be determined. To determine these parameters, the period of interest, T, must be defined explicitly. We define T as the time for the output node (emitter of the emitter follower) to switch $\frac{1}{2}\phi$. Thus,

$$\psi_e = \frac{1}{2}\phi \tag{4.24}$$

It is very important to note that a $\frac{1}{2}\phi$ voltage change at the emitter of the emitter follower does not imply a $\frac{1}{2}\phi$ voltage change at the base of the emitter follower. Voltage change at the base

will depend on the voltage drop across the B-E junction, which in turn, will depend on the base resistance of the transistor. When the output is being charged up, a large amount of excess base current is flowing into the base. Therefore, an excess voltage drop is incurred. A good approximation is

$$\psi_b = \frac{5}{8}\phi \tag{4.25}$$

and i_{RC} can be computed as

$$i_{RC} = \frac{i_{peak} + i_{mid}}{2} \tag{4.26}$$

where i_{peak} stands for the maximum current through Rc and i_{mid} stands for the current at T (the end of the period of interest). Knowing ψb, one can find i_{mid}. Thus, Eq.(4.19) has a value of

$$i_{RC} = \frac{\frac{\phi}{Rc} + \frac{3\phi}{8Rc}}{2} = \frac{0.55}{Rc} \tag{4.27}$$

Substituting Eqs. (4.24) (4.25) and (4.27) into Eq.(4.23), we obtain the final expression.

$$T = 0.455R_c C_t - \tau_f \tag{4.28}$$

$$+ \sqrt{0.207(R_c C_t)^2 + 0.911\tau_f R_c C_t + 1.457\tau_f R_c C_{load} + \tau_f^2}$$

Equation (4.28) is a complete expression for the complex actions of emitter follower charge-up. In fact, both the I-V conversion delay and emitter follower delay can be evaluated by it. Now we are ready to incorporate the effects of the loading resistance, Rf, into the charge-up delay. We shall drop the approximation of Eq.(4.17), and replace it by

$$i_e = i_{cload} + i_{Rf} \tag{4.29}$$

Substituting Eq.(4.29) into Eqs.(4.15) and (4.16), one obtains

$$\frac{i_{Rc}}{2\tau_f}T^2 - \left(\frac{C_t \psi_b}{2\tau_f} - i_{Rc} + i_{Rf}\right)T - (C_t \psi_b + C_{load}\psi_e) = 0 \tag{4.30}$$

A valid approximation for the average increase of current through Rf is

$$i_{Rf} = \frac{1}{4}\frac{\psi_e}{Rf} \tag{4.31}$$

Substituting Eqs.(4.24), (4.25), (4.27) and (4.31) into Eq.(4.30) and solving the quadratic equation again, one obtains

$$T = 0.455R_c C_t - \tau_f + f_1(R_f) \tag{4.32}$$

$$+ \sqrt{0.207(R_c C_t)^2 + 0.911\tau_f R_c C_t + 1.457\tau_f R_c C_{load} + \tau_f^2 + f_2(R_f)}$$

$$f_1(R_f) = \frac{0.3637\tau_f R_c}{R_f} \tag{4.33}$$

$$f_2(R_f) = \frac{\tau_f R_c}{R_f}(0.331C_t R_c^2 - 0.727\tau_f + \frac{0.132\tau_f R_c}{R_f}) \tag{4.34}$$

Equation (4.32) is an analytical expression for the extrinsic delay, τ_{ext}. Figure 4.3 compares several *analytical* charge-up waveforms with their corresponding *accurate* waveforms.

It should be pointed out that from Eq.(4.34), τ_{ext} is independent of the base resistance of the emitter follower. Actually, τ_{ext} does have a weak dependence on rb. Specifically, ψ_b of Eq.(4.26) is strongly determined by rb. Thus to incorporate the effects of rb, we can simply replace ψ_b by $\psi_b(rb)$ which is determined approximately by

$$\psi_b(rb) \approx \psi_e + rbi_{b(excess)} \approx 0.4 + rbi_{b(excess)} \tag{4.35}$$

4.3.2. Emitter follower discharge

Again, we consider the equivalent circuit in Fig. 4.2. When the current, I_{tree} is steered to node 1, the voltage at the base of the emitter follower is pulled down at a rate determined by τ_{RcCt} ,which is derived in Eq.(4.1). At the output of the ECL gate (node 3), the voltage also drops at a certain rate, τ_{fall}. Usually, τ_{RcCt} is *not* equal to τ_{fall}. The mechanisms governing the emitter follower discharge can be easily understood from the following three cases.

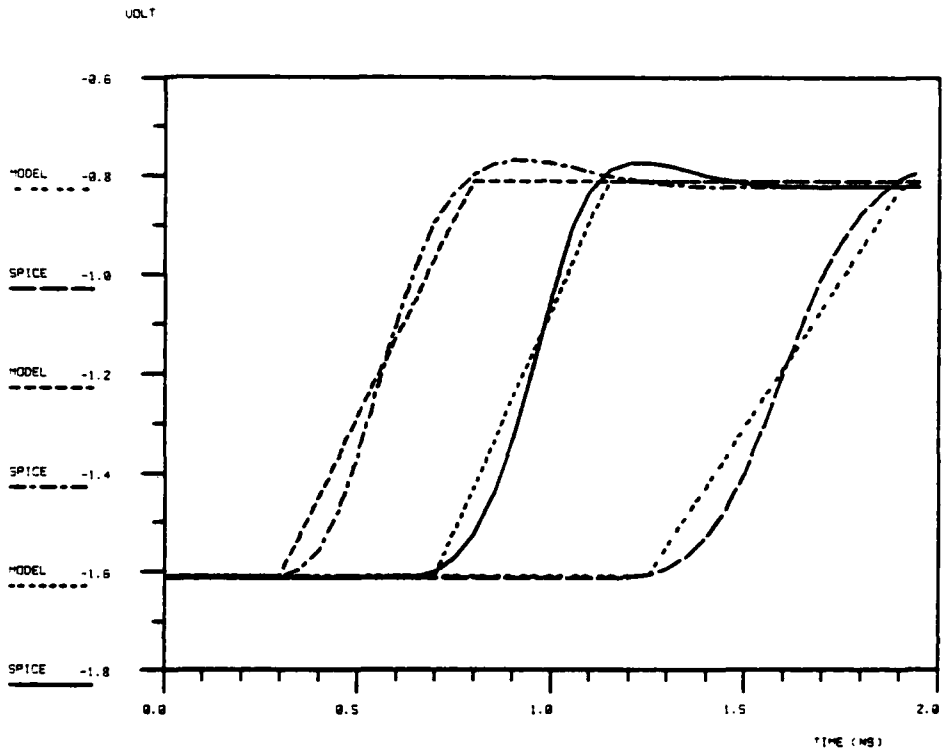

Figure 4.3 Verification of Eq.(4.33)

(1) $C_t << C_{load}$: C_{dif} is quickly discharged by I_{tree}. The emitter follower is effectively turned off. Thus, C_{load} is discharged entirely through Rf . Or, if τ_{load} is the RC time constant at the output, $\tau_{fall} \approx \tau_{load}$.

(2) $C_t >> C_{load}$: Output voltage is completely controlled by τ_{RtCt} ($\tau_{fall} \approx \tau_{RtCt}$). Emitter follower stays on throughout the transient time.

(3) $C_t \approx C_{load}$: τ_{fall} is strongly dependent on both time constants, τ_{RcCt} and τ_{load} .

It is very difficult to derive analytical expressions relating the discharge time to various parameters. The reasons are as follows. First, numerical iteration is necessary to determine the $i_{b(excess)}$ flowing out of the base region. Second, during the transient, the discharge mechanism can

switch among any of the three cases described above, and thus, make it difficult to predict the waveforms.

By keeping in mind the three limiting cases above, expressions can be logically *formulated* and verified by data obtained from SPICE. The discharge mechanism can be shown to obey

$$\tau_{fall} \approx \frac{\tau_{RcCt}(1 + 0.9\alpha) + \tau_{load}\,\alpha^2}{1 + \alpha^2} \tag{4.36}$$

where

$$\tau_{RcCt} = 0.693 R_c C_t \tag{4.37}$$

is the discharging time constant at the base of the emitter follower, and

$$\tau_{load} = R_f\, C_{load}\, ln\,(\frac{VEE - \phi}{VEE - 1.5\phi}) \tag{4.38}$$

is the discharging time constant at the output of the ECL gate, and can be evaluated given the output swing (ϕ) and VEE. For VEE of 5V and ϕ of 0.8V,

$$\tau_{load} = 0.100 R_f\, C_{load} \tag{4.39}$$

In Eq.(4.36)

$$\alpha = \frac{\tau_{load}}{\tau_{RcCt}} \tag{4.40}$$

When $C_t << C_{load}$, from Eq.(4.36), $\tau_{fall} \approx \tau_{load}$. When $C_t >> C_{load}$, $\tau_{fall} \approx \tau_{RtCt}$. When $C_t \approx C_{load}$, τ_{fall} can be shown to depend on C_{load} quite linearly. Thus, all three cases discussed above are satisfied by Eq.(4.36). Figure 4.4 compares several analytical discharge waveforms with their corresponding SPICE results.

4.4. Summary

From Eq.(4.32) and Eq.(4.36), we see that τ_{fall} can be expressed as

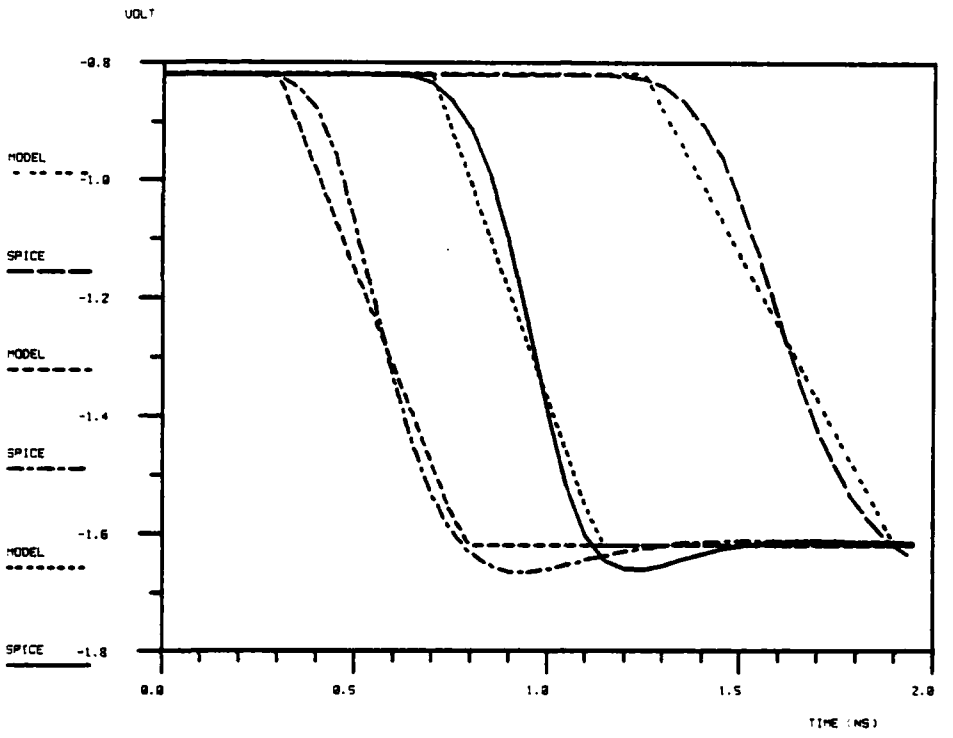

Figure 4.4 Verification of Eq.(4.33)

$$\tau_{ext} \approx f_{ext}(C_{jc}, C_{ccs}, C_{jc}f, C_{load}, Rc, Rf, \tau_f)_{first-order} \tag{4.41}$$

Together with the expressions derived for the intrinsic delay, namely,

$$\tau_{in} \approx f_{in}(rb, \tau_f, Rc, C_{croot}, T_{slew})_{first-order} \tag{4.42}$$

we can then described the complete delay of ECL circuit as

$$\tau_d \approx F_d(\tau_f, rb, Rc, C_{jc}, C_{cs}, C_{croot}, C_{jc}f, T_{slew}, Rf, C_{load})_{first-order} \tag{4.43}$$

Equation (4.43) is indeed what we obtained from (Eq. 2.19). From Fig. 3.7, we can thus find the threshold crossing time from

$$t_2' = t_1' + \tau_{in} + \tau_{ext} \tag{4.44}$$

This sums up our discussion on the delay model for a single-input, single-level ECL gate. In the next chapter this model will be extended to cover more complicated circuits.

CHAPTER 5

MORE COMPLEX ECL LOGIC STRUCTURES

5.1. Introduction

In order to make our approach more useful, it is necessary to derive delay functions for more complex logic structures. Figure 5.1 shows a logic realization of (A+B+C)(D+E) and its complement. The novel features are apparent as compared with a single-level, single-input gate. Two transistors have their emitters tied together to form an "OR" logic and a stack logic realization is used to generate two levels of functional complexity (AND) per bias current. This circuit has an efficient use of both power and device areas. The penalty is that two bias voltage levels are required. As we will see below, the critical timing for this type of complex ECL gates can be obtained by extending the basic delay model derived in the previous two chapters.

Other complex ECL structures that do not resemble the regular multiple level and multiple input circuit (Fig. 5.1) are certainly possible for more efficient implementation of complex logic functions. Yet, from the delay point of view, the switchings of these complex ECL structures bear the same timing characteristics as the regular multiple input and multiple level structure. For example, a special ECL structure shown in Fig. 5.2 can realize the EXCLUSIVE OR and its complement logic. In terms of switching delay, it is merely a simple two-level ECL circuit with timing characteristics similar to a NAND gate.

5.2. Timing constraints for single-input, multilevel circuits

Figure 5.3 shows a simple two-level ECL AND (NAND) gate for inputs A, B. Two reference voltages, VRS1 and VRS2 are needed for proper operations. VRS2 can be implemented by a diode level shift from VRS1, or

$$VRS\,2 = VRS\,1 + \phi \tag{5.1}$$

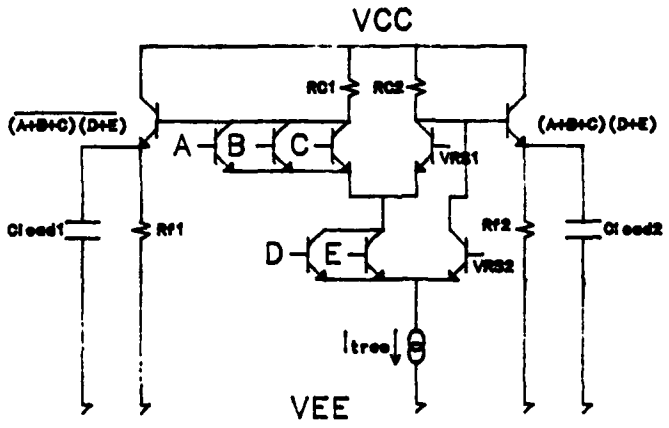

Figure 5.1 A logic realization of (A+B+C)(D+E) and its complement

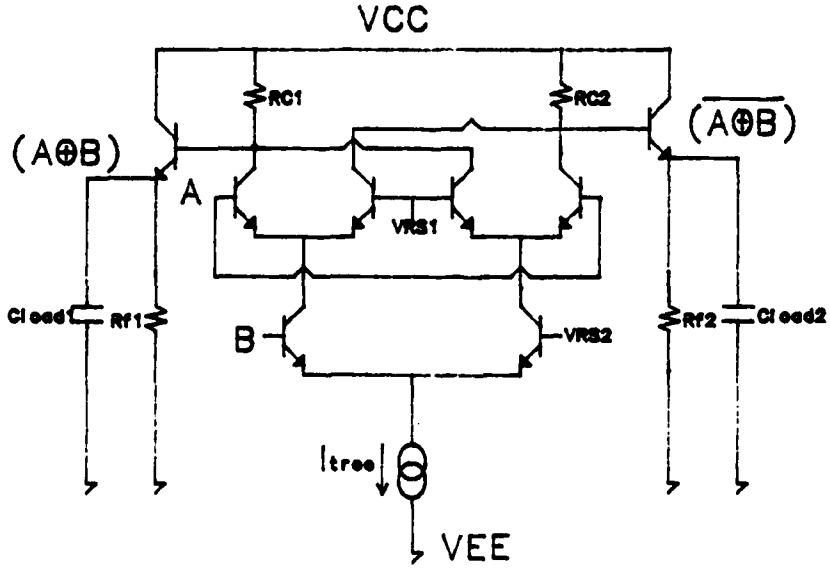

Figure 5.2 A logic realization of EXCLUSIVE OR and EXCLUSIVE NOR

When both inputs A and B switch to "HIGH" (V_A = -0.8, V_B = -1.6), I_{tree} is steered to the load resistor R1 through Q1 and Q3. Thus, V1 (V2) is "LOW" ("HIGH"). When any one of the two inputs is low, I_{tree} is steered away to the load resistor R2.

A simple analogy can be used to illustrate the delay through a stacked circuit. Consider the *electrons* moving through *transistors* as *water molecules* flowing through *valves*. The flow of these molecules can be regulated by a valve that either opens or closes passage. Associated with each valve there is an opening time and a closing time. These are times to turn on or to turn off a valve. We denote these times as τ_{valve}. At a junction of valves, these molecules will seek passage through the opened valves. We will assume that between valves a molecule takes no time to travel since there are plenty of spaces for it to move around. However, at an opened valve, it will have to wait in line with other fellow molecules to pass through the narrow passage provided. We denote this waiting delay as $\tau_{transit}$. A path from the bottom valve to the top valve is called a *branch*. A

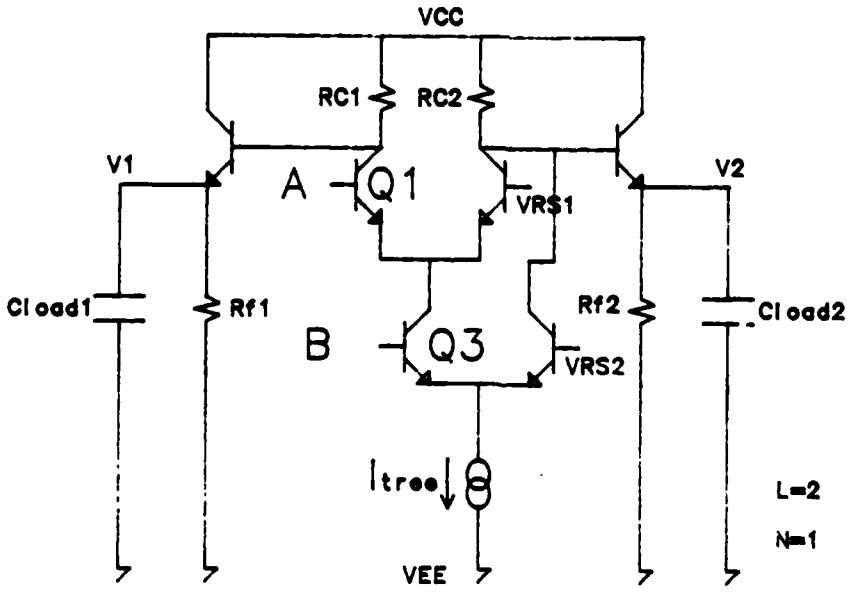

Figure 5.3 A simple two-level ECL gate

junction of valves is called a *node*.

From this analogy, we define for the i^{th} level (for a two-level circuit, the top level is level 1 and the bottom level is level 2),

$$\tau_{valve}(i) = \tau_{in}(i) \tag{5.2}$$

where $\tau_{in}(i)$ is the intrinsic delay associated with the i^{th} level, and

$$\tau_{transit}(i) = \gamma \tau_f(i) \tag{5.3}$$

where γ is an empirical number and is approximately equal to 0.70 from SPICE results. Since τ_f (the forward transit time) is constant for a given circuit, $\tau_{transit}$ is constant for every level.

5.2.1. Single input switching

In this section we consider that only one input (all other inputs remain "HIGH") is switching in a stacked circuit. The total intrinsic delay is indicated as τ_{IN} and can be found by inspection from Eq.(5.2) and Eq.(5.3). If the switching input is at level i,

$$\tau_{IN} = \tau_{valve}(i) + (i-1)\tau_{transit} \tag{5.4}$$

or

$$\tau_{IN} = \tau_{in}(i) + \gamma(i-1)\tau_f \tag{5.5}$$

For a stacked circuit, the extrinsic delay (τ_{EXT}) is associated only with the top level. Therefore, results obtained in Chapter 4 can be applied directly.

$$\tau_{EXT} = \tau_{ext} \tag{5.6}$$

and the threshold crossing time, τ_{cross}, is given by

$$\tau_{cross} = t_1' + \tau_{IN} + \tau_{ext} \tag{5.7}$$

where $t_1' = t_{th}$ (Fig. 3.7).

5.2.2. Simultaneous switching

When more than one input change simultaneously, the situation is more complex since the inputs can be applied at different times and with different slew rates. However, it will be shown in this section that using the *valve analogy* described before, the extension to this case is rather natural.

5.2.2.1. All inputs from low to high

Here we consider that all inputs change simultaneously from "LOW" to "HIGH". From the *valve analogy*, molecules can flow unobstructed through an entire branch only when *all* the valves associated with this branch are opened. As a result, τ_{IN} for the whole stacked circuit is mainly limited by the **slowest** intrinsic midpoint crossing time, $t_2'(k)$, at the k^{th} level. $t_2'(i)$ is the time when V(1) or V(2) in Fig. 5.3 crosses the threshold voltage for an intrinsic circuit due to an input change at level i (assuming all other inputs are fixed). From results obtained in Section 3.4, and Eq.(5.5), we obtain

$$t_2'(i) = t_1'(i) + \tau_{in}(i) + \gamma(i-1)\tau_f \tag{5.8}$$

for the i^{th} level and

$$\tau_{cross} = \tau_{ext} + max(t_2'(i)) \tag{5.9}$$

Obviously, the output will begin to switch (t_1') only after the latest input begins to switch. Therefore,

$$t_1' = max(t_1'(i)) \tag{5.10}$$

Note that Eqs.(5.9) and (5.10) are applicable to any number of levels, L.

5.2.2.2. Multiple inputs from high to low

In this section we consider that when more than one input switching from "HIGH" to "LOW." The case when only one input is switching has already been covered in Section 5.2.1. From the

valve analogy, molecules can be redirected to other branches by turning off *any* valve associated with the current branch. Thus, an estimate of the timing constraint is obtained by choosing the fastest intrinsic midpoint crossing time. Therefore,

$$\tau_{cross} = \tau_{ext} + min\,(t_2'(i)) \tag{5.11}$$

and the output will begin to switch as soon as any input begins to switch or

$$t_1' = min\,(t_1'(i)) \tag{5.12}$$

Equation (5.11), in fact, provides the worst-case timing prediction for multiple inputs that are switching simultaneoulsly. It assumes that during switching *all* the molecules are redirected to the other branch from valve(k), at the k^{th} level, which turns off faster than any other valve. In reality, there can be an *overlapping time* between each of the other valves and valve(k). Therefore, the molecules can be redirected to other branchs through other valves as well. Let us denote $\tau_{ovlap}(i)$, $i = 1,2,\cdots,L-1$, as the overlap time between each individual valve along the branch to valve(k). L is the total number of levels. Note that $\tau_{ovlap}(i)$ ranges from 0 to $\tau_{in}(k)$. To account for this reduction of delay, we rewrite Eq.(5.11) as

$$\tau_{cross} = \tau_{ext} + min\,(t_2'(i)) - \sum_{i=1}^{L-1}\Big(\sum_{j=0}^{i}\Big)^{-1}\Big(\frac{\tau_{ovlap}(i)}{2}\Big) \tag{5.13}$$

Note that Eq.(5.13) is valid only when $\tau_{ovlap}(i)$ is decreasing in value for each increment of i. This can be done by simply sorting $\tau_{ovlap}(i)$. Equation (5.13) is a powerful expression. The reasons are

(1) The number of level, L, is arbitrary.

(2) Any combination of inputs switching from "HIGH" to "LOW" simultaneously is allowed.

(3) Inputs can switch at different times with different slew rates.

(4) It can be easily implemented in a computer program.

5.3. Timing constraints for multiple inputs, single level circuits

Figure 5.4 shows a simple three-input ECL "OR" ("NOR") gate for inputs A, B, C. When one or more inputs switch to "HIGH," I_{tree} will be steered to the load resistor $R1$. When all the inputs are "LOW," the current path is through the branch of $R2$.

5.3.1. Single input switching

We consider only one input is switching while all other inputs are "LOW". The timing model is identical to the one we derived earlier for a basic gate. However, since there is more than one input, multiples of cjc (base-collector feedback capacitor) must be added to compute τ_{ext}.

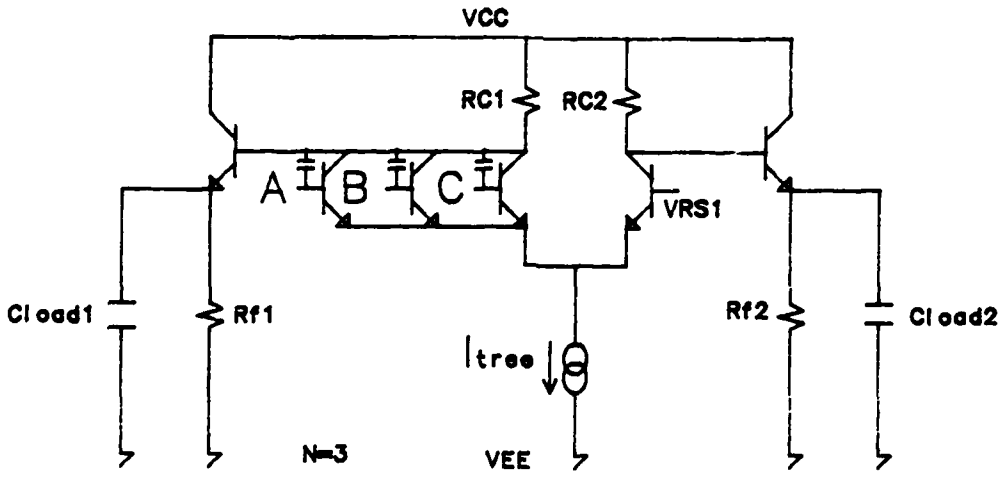

Figure 5.4 A three-input ECL gate

5.3.2. Simultaneous switching

When more than one input change simultaneously, the situation is more complex since the inputs can be applied at different times and with different slew rates. However, the timing model derived for the multilevel circuits can be applied here directly.

5.3.2.1. Multiple inputs from low to high

In this section we consider the case when there are more than one input that are switching from "LOW" to "HIGH." The case when only one input is switching has already been covered in Section 5.3.1. From the *valve analogy*, molecules can be directed to a branch by turning on *any* valve associated with the current branch. Thus, an estimate of the timing constraint is obtained by choosing the **fastest** intrinsic midpoint crossing time, $t_2'(k)$ for valve(k). However, some molecules can also flow to this branch through other valves, valve(n), associated with this node as long as there is a non-zero input overlapping time, $\tau_{ovlap}(n)$, with valve(k). Let N equal the total number of parallel inputs associated with the node in question. We can also derive an equation similar to Eq.(5.13).

$$\tau_{cross} = \tau_{ext} + min(t_2'(n)) - \sum_{n=1}^{N-1}(\sum_{j=0}^{n})^{-1}(\frac{\tau_{ovlap}(n)}{2}) \qquad (5.14)$$

$t_2'(n)$ is defined as the midpoint crossing time for valve(n) when all other valves at the same node are "LOW," or

$$t_2'(n) = t_1'(n) + \tau_{in}(n) \qquad (5.15)$$

Note that Eq.(5.14) is valid only when $\tau_{ovlap}(n)$ is decreasing in value for each increment of n. This can be done by simply sorting $\tau_{ovlap}(n)$.

Equation (5.14) is a powerful formula for computing the timing constraint for any number of parallel inputs, N, when any combination of inputs is switching from "LOW" to "HIGH" at different times with different slew rates. The output will begin to switch (t_1') as soon as any input

begins to switch. Therefore,

$$t_1' = min\,(t_1'(i)) \tag{5.16}$$

5.3.2.2. All inputs from high to low

Here we consider that all inputs change simultaneously from "HIGH" to "LOW." From the *valve analogy*, molecules cannot flow through a branch unless *all* the valves associated with this branch are opened. As a result, τ_{IN} for the whole stacked circuit is mainly limited by the **slowest** intrinsic midpoint crossing time, $t_2'(k)$ at the k^{th} input. Therefore,

$$\tau_{cross} = \tau_{ext} + max\,(t_2'(i)) \tag{5.17}$$

Obviously, the output will begin to switch (t_1') only after the latest input begins to switch, or

$$t_1' = max\,(t_1'(i)) \tag{5.18}$$

5.4. Interconnection delay

So far in our discussion, all results are based on the analysis of a single ECL gate with inputs driven by voltage sources. In the actual environment, *interconnections* between gates play an important role in delay analysis.

Interconnection delay can be accounted for by a simple lumping of all capacitances connected to the output of each gate, or

$$C_{lump} = C_{load} = C_{wiring} + C_{fanout} \tag{5.19}$$

where C_{wiring} stands for the metal wiring capacitances. C_{fanout} stands for the capacitances associated with the gates connected to that particular output. C_{wiring} should be either specified by users or inputted from layout extraction program. C_{fanout} can be determined by summing all associated capacitances (C_{jc} and C_{je}) for each fanout.

For the purpose of achieving high speed, metal is the only material used to provide interconnections for bipolar integrated circuits. As a result, there is negligible wiring resistance.

CHAPTER 6

IMPLEMENTATION

The timing model described in Chapters 3 to 5 has been implemented in a computer program. We now evaluate the performance of our timing model based on its computational speed and accuracy.

The first example consists of several *perturbation* tests. We perturb one delay- sensitive parameter one at a time while keeping the rest of the parameters constant. Then, we compare the *change* of delays for each set of perturbations with those from SPICE. This is an extremely critical way of verifying our model since error cancellations are kept to a minimum. Three sets of perturbations are evaluated for three critical parameters, Rc, Ccs and Cload. The results are shown from Fig. 6.1 to Fig. 6.3 at the end of this chapter.

The second example is a chain of identical inverters. This test is valuable for evaluating the effects of input slew rate. If the error does not grow as a function of gates, we can say that the timing model can handle input slew rate very well. Figure 6.4 shows the waveforms for a 25-

Table 6.1 CPU seconds taken for a chain of inverters

Number of Inverters	CPU Seconds	
	SPICE	MODEL
5	24.23	0.20
10	44.84	0.34
15	71.4	0.58
20	231.84	0.89
30	634.08	1.44
50	2664.65	2.46

inverter-chain at different outputs (V6, V15, V26). Note that the error does not grow throughout the entire chain. In Table 6.1 the total job times taken by SPICE and the timing model are provided for comparison. Note that for large circuits the timing model can be three orders of magnitude faster than that for SPICE.

The third example is a one-bit full-adder circuit. The logic diagram is shown in Fig. 6.5. Inverters are purposely included to allow our simulations to cover more varieties of ECL structures.The input waveforms for x, y and z are shown in Fig. 6.6. Figures 6.7 and 6.8 compared the results of the sum bit and carry bit respectively. Note that the accuracy is generally within 10% as compared to that for SPICE. This example demonstrates the capability of our timing model to handle complex structures like the NAND, NOR, and EXCLUSIVE OR gate.

Our last example is a random logic shown in Fig. 6.9 with multiple inputs and multiple level gates. When inputs in Fig. 6.10 are applied, inputs to the last OR gate switch simultaneously at different starting times with different slew rates (shown in Fig. 6.11). The compared results of output at node 9 are shown in Fig. 6.12. This example demonstrates the capability of our timing model to handle gates with multiple inputs that can switch simultaneously with different slew rates.

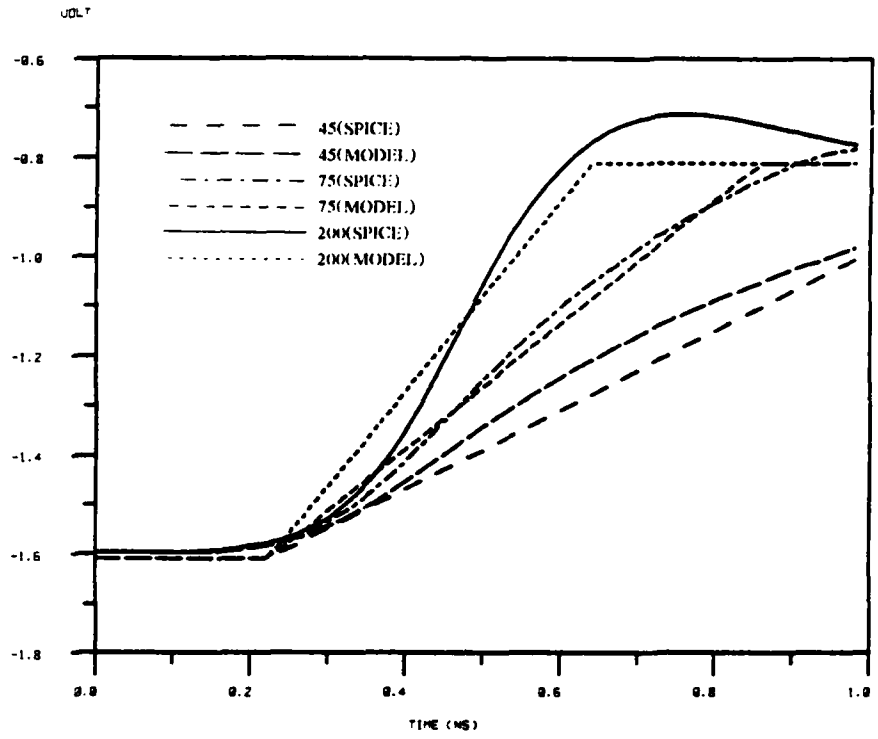

Figure 6.1 Perturbations of circuit parameter Rc

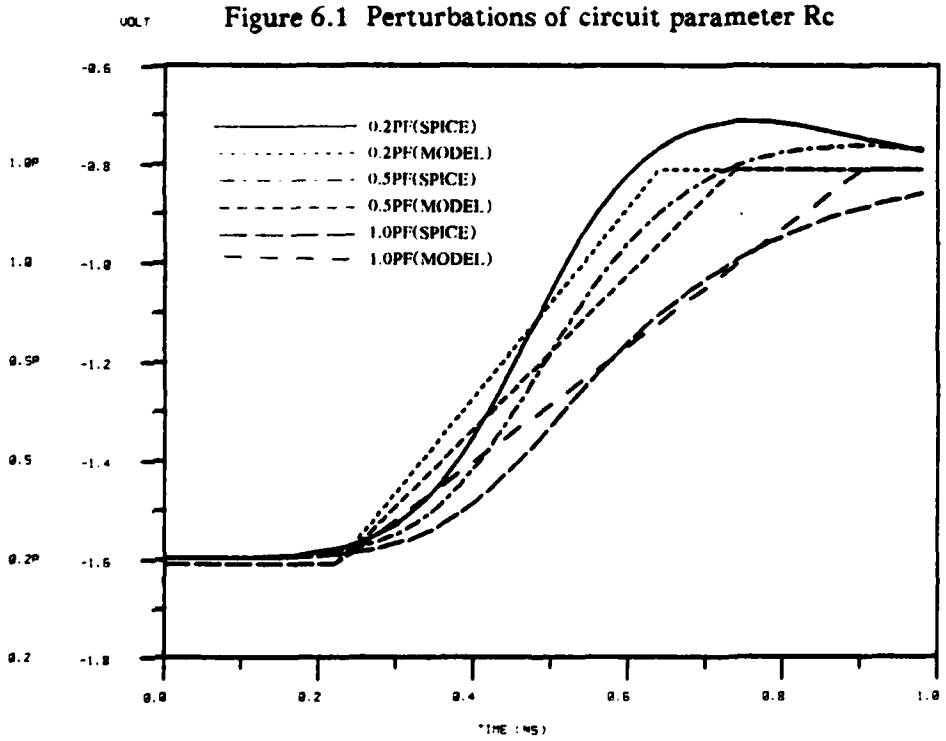

Figure 6.2 Perturbations of device parameter Ccs

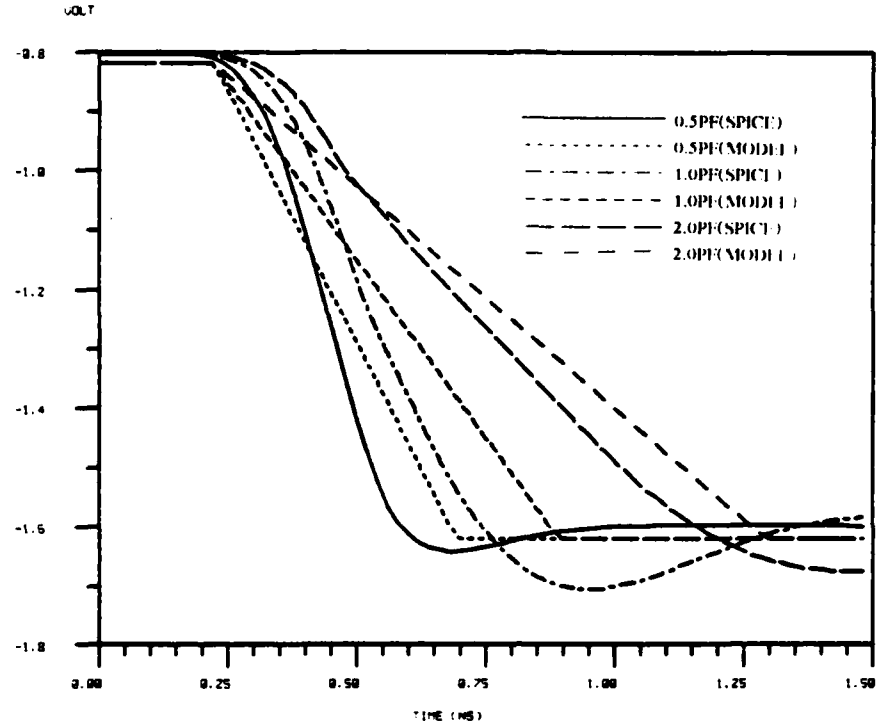

Figure 6.3 Perturbations of device parameter Cload

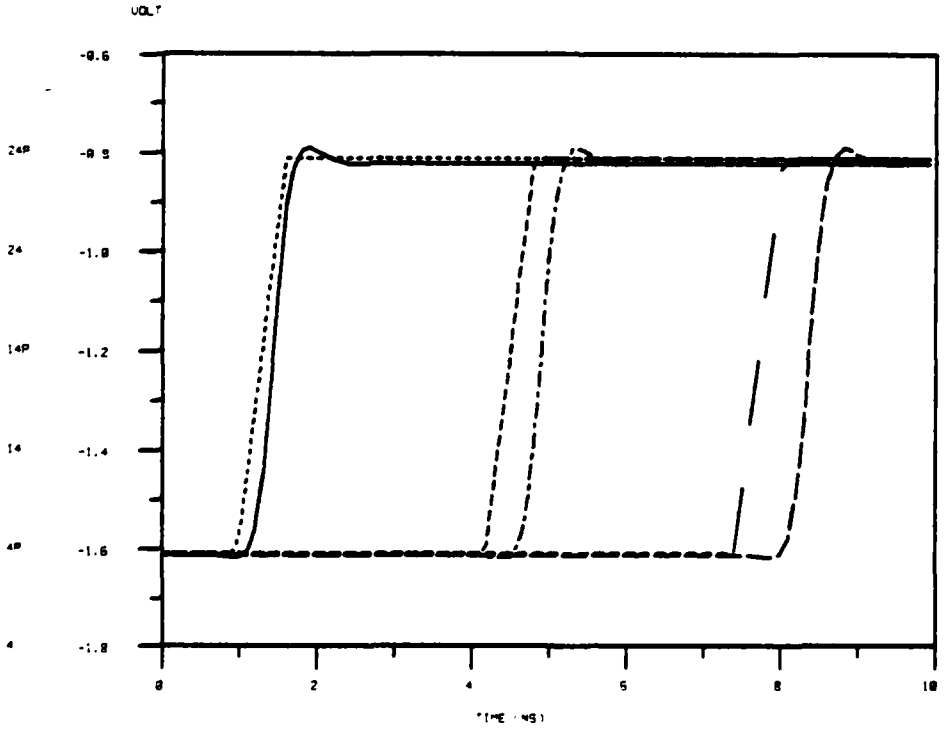

Figure 6.4 Inverter-chain results at the 4^{th} , 14^{th} and 24^{th} gate

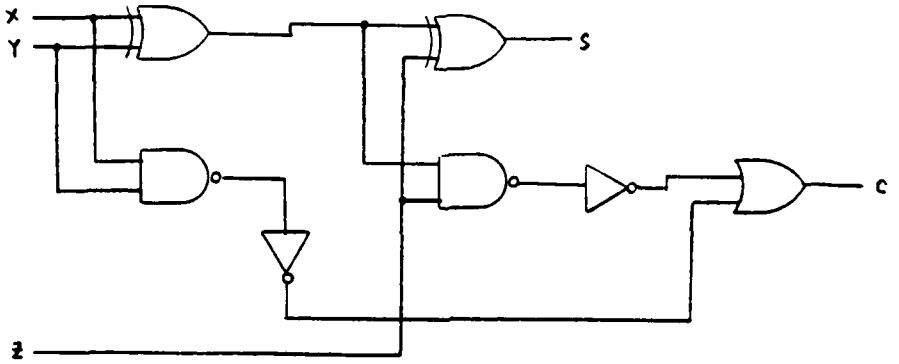

Figure 6.5 Logic diagram of a one-bit full-adder

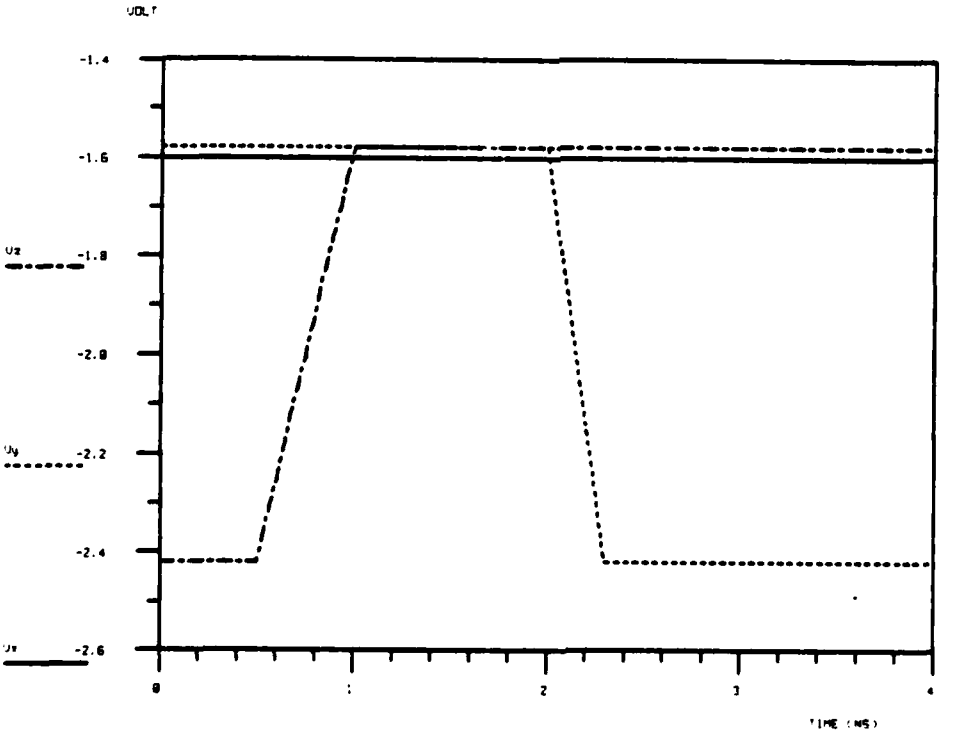

Figure 6.6 Inputs to the one-bit full-adder

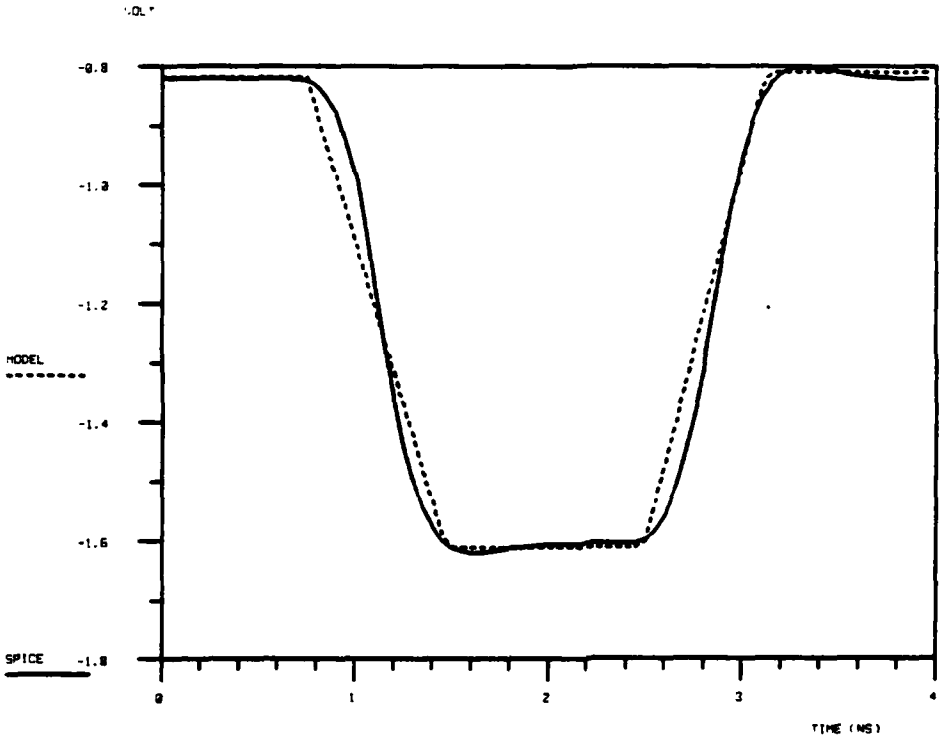

Figure 6.7 Waveforms for the sum bit

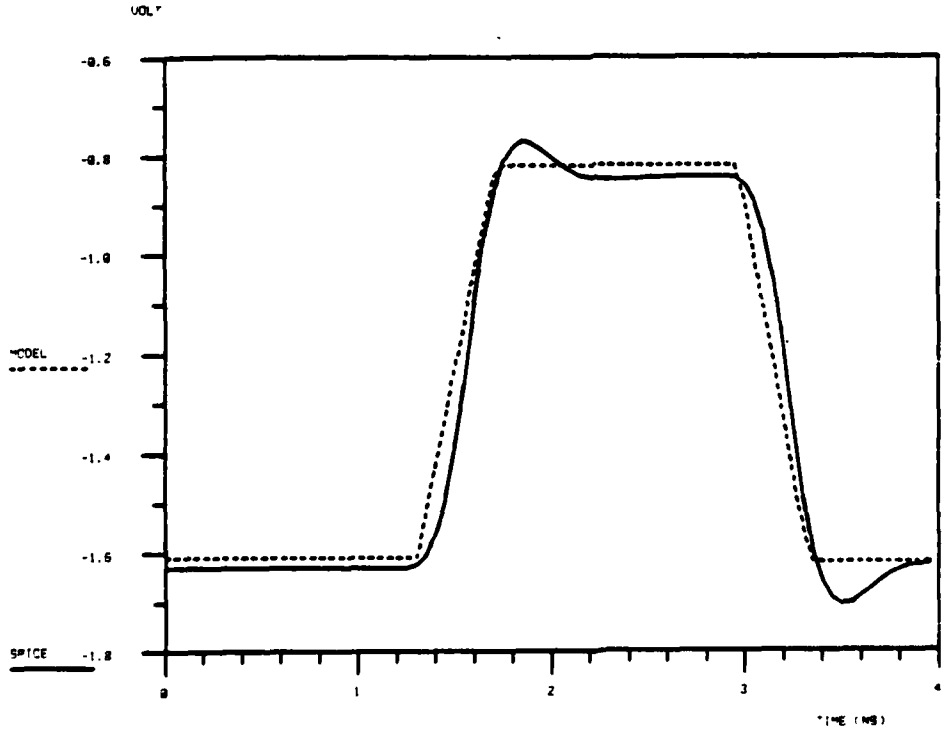

Figure 6.8 Waveforms for the carry bit

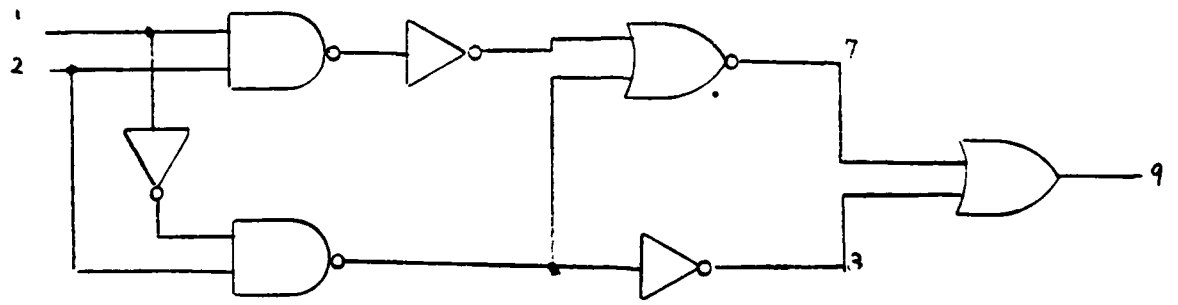

Figure 6.9 Random logic

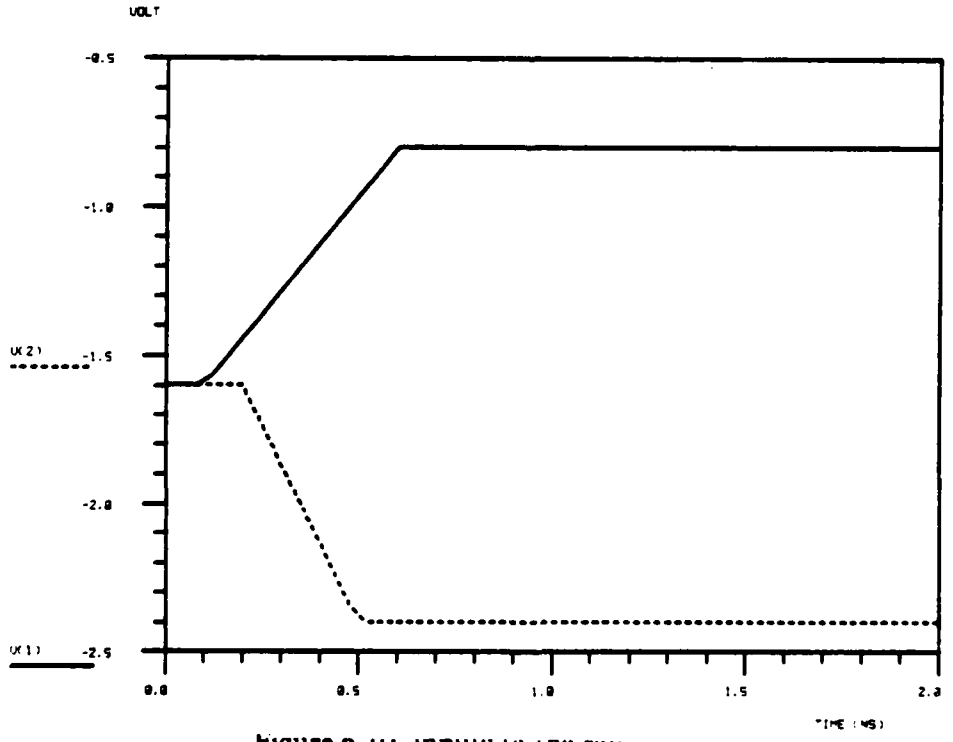

Figure 6.10 Inputs to the random logic

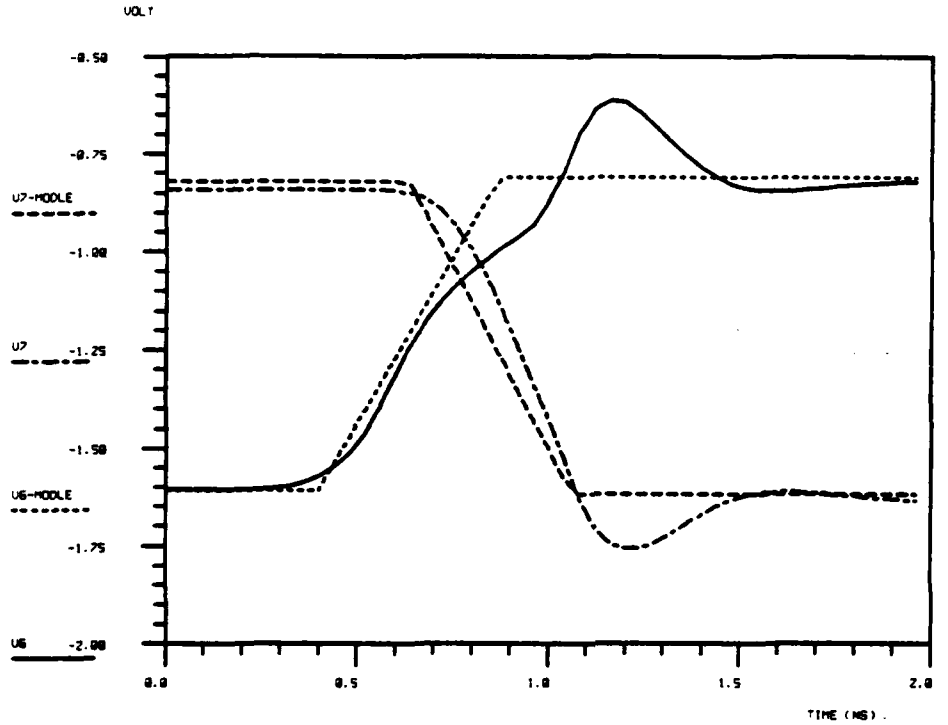

Figure 6.11 Voltage comparison of node 7,8 of circuit shown in Fig. 6.9

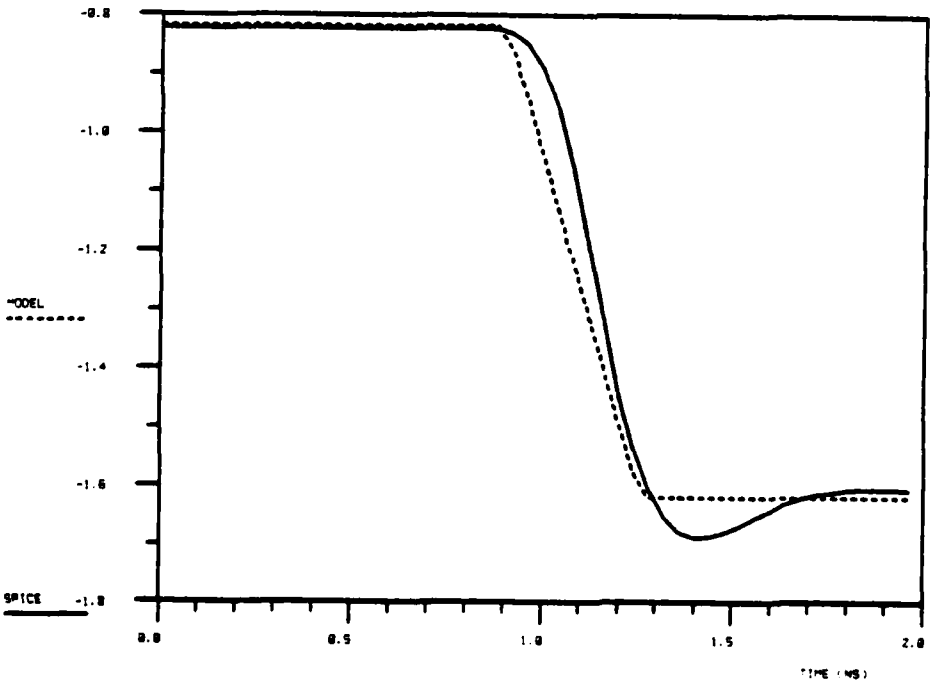

Figure 6.12 Voltage comparison of node 9 of circuit shown in Fig. 6.9

CHAPTER 7

CONCLUSIONS

Conventional circuit simulators such as SPICE predict both steady-state and transient response very accurately, but are cost effective for circuits containing a few hundred transistors or less. A switch-level approach to simulate the steady-state bipolar ECL circuit has been proposed and implemented. It provides accurate logic information at reasonable simulation cost for large circuits of any complexity. In this thesis we have described a timing model which can be used to provide fast and fairly accurate timing information for high-speed ECL circuits. Our timing model requires *no* preprocessing since analytical expressions are derived to model the dynamic properties of the circuits. We also demonstrate the extensions of our model to more complex circuits with multiple inputs and multiple levels.

In Chapter 2, we found that the switching delay for a basic ECL gate has strong dependences on ten device and circuit parameters. We then decomposed the delay into separate stages. The delay function for each stage depends on only a few parameters. We mainly decompose the delay into **intrinsic delay, I-V conversion delay** and **buffer delay**. Charge-control models for device under forward-biased and cutoff mode are also given in this chapter. These models are crucial to our analysis of switching delay in later chapters.

In Chapter 3, the expressions governing the intrinsic delay are derived. The important effect of input slew-rate is also incorporated. We found that the intrinsic delay is directly related to the amount of minority charges stored in the base region. Input base currents during the transient response provide the main mechanisms to extract or inject these minority charges. For a low-power device, the stored base charges are relatively low and thus require less time to switch intrinsically. Moreover, the small size of a low-power transistor reduces the parasitic base resistance and results

in a significant increase of transient base current.

Even though intrinsic delay can be kept to a minimum by lowering the the power of a gate, it is shown in Chapter 4 that there exists an important trade-off. We lump the I-V conversion delay and buffer delay together and call it **extrinsic delay**. The extrinsic delay is directly related to the amount of majority charges stored in the depletion capacitors. To charge or discharge these parasitic capacitors rapidly requires a great deal of current (power). Therefore, in general, one wants to increase the power to reduce the extrinsic delay. Unfortunately, the large size of a high power transistor increases considerably the values of all the parasitic capacitors.

When we combine the analytical expressions derived for the intrinsic and extrinsic delays of a basic gate, we come up with equations that express their dependences on the ten parameters we first observed. In Chapter 5 the timing model is extended to include more complex circuits with multiple or/and multiple levels. Our results show that the extensions are rather natural and valid for any given number of inputs or levels. Therefore, the dynamic properties of circuits of any complexity can be properly explained via our timing model.

The switching delays of a number of ECL circuits have been evaluated using our timing expressions in the first part of Chapter 6. The performances based on their computational speed and accuracy are compared with the results simulated by SPICE. It is found that in general the simulation cost of our timing model is almost negligible compared with that of SPICE. For large circuits of more than a thousand transistors, our timing model can run up to three or four orders of magnitude faster than SPICE, yet the timing informations provided by the timing model are in general accurate within 15% when compared with that for SPICE. It should be pointed out here that most of the expressions derived in this thesis are based on the models that are pertinent and assumptions are made to reduce our expressions into compact equations that need no iterations. We do not use SPICE results to extract or fine tune the coefficients of our delay equations.

We now consider several extensions that are made possible from our timing model. In general, for integrated circuits of any technology there exists an engineering trade-off between the area and the performance. In short, this trade-off can be described briefly as follows. The current handling capability of an active device is directly proportional to its physical device size. To achieve better performance by pumping in more power, one, therefore, increases the size of the circuit. Similarly, to achieve a higher level by minimizing the size of each individual, one could degrade the performance of the circuit. A good design means that for given constraints on power and area, the performance is minimum. For bipolar ECL high-speed circuits, the steady-state power of each gate is determined mainly by the two circuit parameters, R_c and R_f . Given the output swing, the value of R_c determines the steering current. The power required for the emitter follower (buffer) depends on the value of R_f . The values of the parasitic device parameters such as rb , C_{cs} , C_{jc} can be evaluated for given sizes of transistors provided that the device modeling for a given technology is done properly. For practical design considerations, the size of a transistor is determined entirely by the amount of current it needs to handle. Usually, the rule of thumb is 100 μA per 1 μm emitter width. In view of this, the values of the parasitic device parameters are direct functions of R_c and R_f . Therefore, from the timing expressions derived in this thesis, we can conclude that $\tau_d \approx f\ (R_c, R_f\ )$. Optimization of τ_d with respect to R_c, R_f can then be obtained easily for each gate.

Another important high-speed bipolar logic family is the Emitter-Function-Logic (EFL) [6]. The main feature of a EFL logic is an increase in logic functionality without much increase in circuit complexity as compared to conventional ECL circuits. From the logic point of view, EFL can be viewed as a repartitioned form of ECL as shown in Fig. 7.1 [3]. The input now is at the emitter of the fixed-biased switching transistor. The output is at the emitter of the output transistor. From the delay point of view, EFL circuits are very much similar to ECL circuits. Both of them utilize a constant current source to provide high-speed current switching. One major difference is that the emitter follower (buffer) transistor in an ECL logic gate now acts as one of the switching

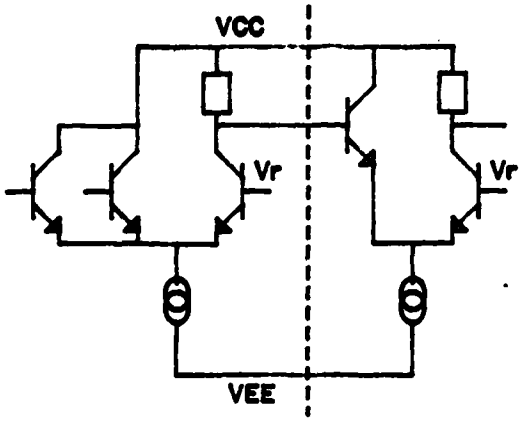

Figure 7.1 Basic EFL gate

transistors for the following gate. Only minor modifications are needed to extend our ECL timing expressions to EFL circuits. In Chapter 4, we defined the extrinsic delay (τ_{ext}) as the lumped sum of the I-V conversion delay and the buffer delay. Since for EFL logic the buffer transistor is eliminated, we can redefine our extrinsic delay as just the I-V conversion delay, which is described in the beginning of Chapter 4. The timing model we derived in this thesis for multiple inputs and can be extended to more complex EFL circuits as well.

An approach similar to the one used in this thesis can be also applied to a special circuit scheme in MOS technology called Source-Coupled-Logic (SCL) to extract its delay expressions. The effects of input slew rate, however, will pose a major obstacle for accurate delay modeling.

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